# SLOVENSKI STANDARD
# oSIST prEN IEC 61189-2-720:2023

**01-april-2023**

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**Preskusne metode za električne materiale, tiskana vezja in druge povezovalne strukture in sestave - 2-720. del: Odkrivanje napak v povezovalnih strukturah z merjenjem kapacitivnosti**

Test methods for electrical materials, printed board and other interconnection structures and assemblies - Part 2-720: Detection of defects in interconnection structures by measurement of capacitance



**Ta slovenski standard je istoveten z:** **prEN IEC 61189-2-720:2023**

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**ICS:**

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|---|---|
| 31.180 | Tiskana vezja (TIV) in tiskane plošče / Printed circuits and boards |

**oSIST prEN IEC 61189-2-720:2023** **en**

# 91/1832/CDV

COMMITTEE DRAFT FOR VOTE (CDV)

| | |
|---|---|
| PROJECT NUMBER: **IEC 61189-2-720 ED1** | |
| DATE OF CIRCULATION: **2023-02-10** | CLOSING DATE FOR VOTING: **2023-05-05** |
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| IEC TC 91 : ELECTRONICS ASSEMBLY TECHNOLOGY | |
|---|---|
| SECRETARIAT: Japan | SECRETARY: Mr Masahide Okamoto |
| OF INTEREST TO THE FOLLOWING COMMITTEES: | PROPOSED HORIZONTAL STANDARD: ☐ Other TC/SCs are requested to indicate their interest, if any, in this CDV to the secretary. |
| FUNCTIONS CONCERNED: ☐ EMC ☐ ENVIRONMENT ☐ QUALITY ASSURANCE ☐ SAFETY | |
| ☒ SUBMITTED FOR CENELEC PARALLEL VOTING<br>**Attention IEC-CENELEC parallel voting**<br>The attention of IEC National Committees, members of CENELEC, is drawn to the fact that this Committee Draft for Vote (CDV) is submitted for parallel voting.<br>The CENELEC members are invited to vote through the CENELEC online voting system. | ☐ NOT SUBMITTED FOR CENELEC PARALLEL VOTING |



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TITLE:

**Test methods for electrical materials, printed board and other interconnection structures and assemblies – Part 2-720: Detection of defects in interconnection structures by measurement of capacitance**

PROPOSED STABILITY DATE: 2028

NOTE FROM TC/SC OFFICERS:

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

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# Test methods for electrical materials, printed board and other interconnection structures and assemblies – Part 2-720: Detection of defects in interconnection structures by measurement of capacitance

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The text of this International Standard is based on the following documents:

| FDIS | Report on voting |
|---|---|
| XX/XX/FDIS | XX/XX/RVD |

Full information on the voting for the approval of this International Standard can be found in the report on voting indicated in the above table.

This document has been drafted in accordance with the ISO/IEC Directives, Part 2.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

The National Committees are requested to note that for this document the stability date is 2028..

THIS TEXT IS INCLUDED FOR THE INFORMATION OF THE NATIONAL COMMITTEES AND WILL BE DELETED AT THE PUBLICATION STAGE.

# Test methods for electrical materials, printed board and other interconnection structures and assemblies – Part 2-720: Detection of defects in interconnection structures by measurement of capacitance

## 1 Scope

This document provides a method to evaluate specific characteristics of printed boards by measuring the capacitance between conductor traces and a ground plane and can be used for qualitative comparison of a test specimen to a reference board. This method is not intended for quantitative measurements and for assessment of conformity to a specification.

## 2 Normative references

There are no normative references.

## 3 Terms and Definitions

For the purposes of this document, the terms and definitions given in IEC 60194-2 apply. No terms and definitions are listed in this document.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

• IEC Electropedia: available at http://www.electropedia.org/

• ISO Online browsing platform: available at http://www.iso.org/obp



## 4 Objective

For testing electrical characteristics of printed board, generally electrical open/short test that shall measure the resistance between nets is the main test method. This open/short test is possible only to look at the pass/the fail of circuits and not to look for any reliability issues of printed board like as mouse bite, delamination, void, and crack. Therefore, the general electrical shall have a limitation. With the capacitance test method, it shall check the existing reliability issues of printed board and this standardization of the additional electrical test is necessary from the development stage. It is possible to accurately measure the differences in the capacitance values of printed board before and after the reliability test. It is enough for the development stage and reliability testing than in-production testing because of the long test time. If not the probing contact issues, there is no problem with the measurement uncertainty. It is possible to look for the defects lie as open/short, mouse bite, delamination, void, and so on by analysing the test defect nets. For looking for the capacitance test method, it shows the capacitance difference depending on the pad width, pad length, and pad distance as shown in Fig. 1. Fig. 1 shows the defect of mouse bite.

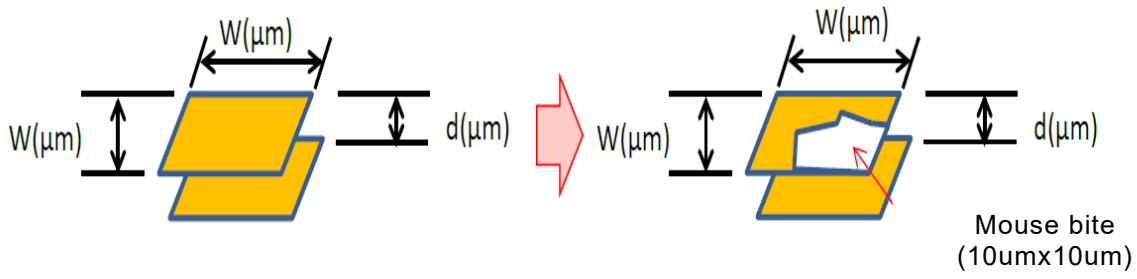



**Figure 1 – The capacitance difference depending on the defect of mouse bite**

## 5 Test specimen

Fig 2 shows the test specimen with top test pads and bottom test pads. It shall be prepared to test the real circuit boards and test coupons with the warpage specification of less than 2 ㎜ for improving the adhesion with the ground metal plate.

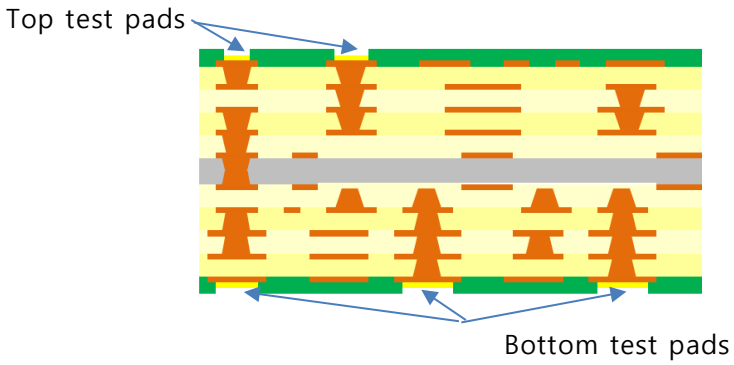
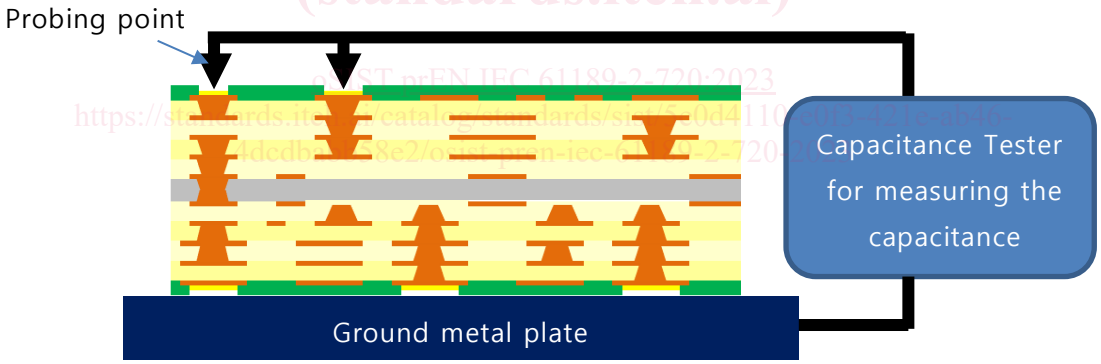



**Figure 2– Test specimen**

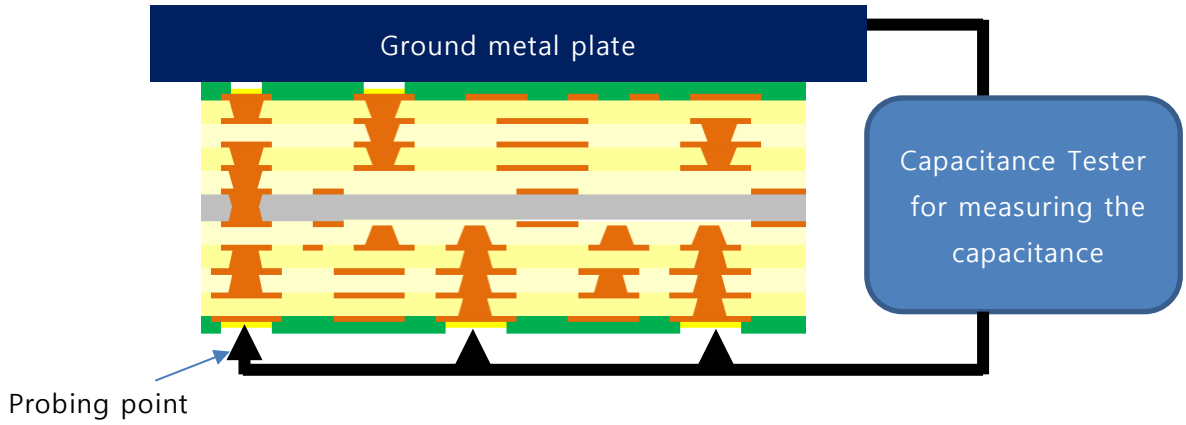
## 6 Test method

Fig. 3 shows the schematic of the capacitance test method for measuring the capacitance using the capacitance tester like as LCR meter and Impedance tester. After contacting the ground metal plate of one side, it shall be tested the capacitance of all of pad of the other side. The top probing tests and the bottom probing tests are conducted.






(a) **Top probing tests for all top pads**




**(b) Bottom probing tests for all bottom pads**

**Figure 3 – Schematic of the capacitance test method**

## 7. Test procedures

The specimen shall be attached on the ground metal plate without any attached materials, and it may need the ground metal plate with the vacuum suction holes for improving the attachment between test specimen and ground metal plate. It shall be connected the 2-port capacitance tester at each probing point and ground metal plate. If looking at the test schematic in Fig. 4, after attaching the test specimen on ground metal plate, the impedance tester with 2-port shall connect to the pads of test specimen and ground metal plate. The ground metal plate shall be the common ground and the capacitance shall measure at each one-side probing point. Also, it needs to measure at each other-side probing point. After that, it shall analyze all of test results by comparing with the average error ratio of all test specimens.

The test sequences to test the capacitance of printed board are as follows.

1) Looking for the reference values with the average value for each test pad by testing 10 specimens, then determining the high limit ratio and the low limit ratio.

2) Cleaning the contamination on the ground metal plate.

3) Putting test specimen on the ground metal plate and attaching the vacuum suction without any attached materials.

4) Firstly, testing the capacitance characteristics of the one-side test specimen with the impedance tester.

5) Repeat the sequence 2).

6) Secondly, attaching the other-side test specimen on the ground metal plate without any attached materials.

7) Testing the capacitance characteristics of test specimen with the impedance tester.

8) Comparing the capacitance characteristics of all of test results with the average error ratio according to high limit and low limit (referred to Annex A).



| A | B | C | D | E | F |
|---|---|---|---|---|---|
| REF-VALUE(F) | MEAS-VALUE(F) | Average error ratio(%) | High LIMIT(%) | Low LIMIT(%) | Judgement (Pass/Failure) |

A = the average capacitance value of 10 times testing values

B = the measured capacitance value

C (%) = (B/A) * 100

F(Pass) range = E ≤ C ≤ D

F(Failure) range = E > C or C > D

9) Judging the pass/the failure for the electrical characteristics of printed board.

## 8. Report

This test method shall include:

a) test schematic for the capacitance test method

b) the impedance tester for measuring the capacitance used

c) the ground metal plate as the common ground used

d) the date of the test

e) the room temperature under which the test was conducted

f) the test sequences

g) high limit and low limit

h) the table of the average error ratio for comparing all of test results

h) the pass/the failure of printed board