SLOVENSKI STANDARD
SIST EN 62326-4-1:2001

01-marec-2001

Printed boards - Part 4: Rigid multilayer printed boards with interlayer connections - Sectional specification - Section 1: Capability Detail Specification - Performance levels A, B and C

Printed boards -- Part 4: Rigid multilayer printed boards with interlayer connections - Sectional specification -- Section 1: Capability Detail Specification - Performance levels A, B and C

Leiterplatten -- Teil 4: Starre Mehrlagen-Leiterplatten mit Durchverbindungen - Rahmenspezifikation -- Hauptabschnitt 1: Bauartspezifikation zum Nachweis der Befähigung - Anforderungsstufen A, B und C

Cartes imprimées -- Partie 4: Cartes imprimées multicouches rigides avec connexions intercouches - Spécification intermédiaire -- Section 1: Spécification particulière d'agrément - Niveaux de performance A, B et C

Ta slovenski standard je istoveten z: **EN 62326-4-1:1997**

ICS:

31.180	Tiskana vezja (TIV) in tiskane ploģ¦e	Printed circuits and boards

SIST EN 62326-4-1:2001 **en**

EUROPEAN STANDARD

NORME EUROPÉENNE

EUROPÄISCHE NORM

EN 62326-4-1

January 1997

ICS 31.180

Descriptors: Printed boards, rigid multilayer, interlayer connections, capability approval, capability detail specification, performance levels A, B and C, capability testing

English version

Printed boards
Part 4: Rigid multilayer printed boards with interlayer connections
Sectional specification
Section 1: Capability Detail Specification
Performance levels A, B and C
(IEC 2326-4-1:1996)

Cartes imprimées
Partie 4: Cartes imprimées multicouches rigides avec connexions intercouches
Spécification intermédiaire
Section 1: Spécification particulière d'agrément
Niveaux de performance A, B et C
(CEI 2326-4-1:1996)

Leiterplatten
Teil 4: Starre Mehrlagen-Leiterplatten mit Durchverbindungen
Rahmenspezifikation
Hauptabschnitt 1: Bauartspezifikation zum Nachweis der Befähigung
Anforderungsstufen A, B und C
(IEC 2326-4-1:1996)

This European Standard was approved by CENELEC on 1996-12-09. CENELEC members are bound to comply with the CEN/CENELEC Internal Regulations which stipulate the conditions for giving this European Standard the status of a national standard without any alteration.

Up-to-date lists and bibliographical references concerning such national standards may be obtained on application to the Central Secretariat or to any CENELEC member.

This European Standard exists in three official versions (English, French, German). A version in any other language made by translation under the responsibility of a CENELEC member into its own language and notified to the Central Secretariat has the same status as the official versions.

CENELEC members are the national electrotechnical committees of Austria, Belgium, Denmark, Finland, France, Germany, Greece, Iceland, Ireland, Italy, Luxembourg, Netherlands, Norway, Portugal, Spain, Sweden, Switzerland and United Kingdom.

CENELEC

European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

Central Secretariat: rue de Stassart 35, B - 1050 Brussels

Foreword

The text of document 52/656/FDIS, future edition 1 of IEC 2326-4-1, prepared by IEC TC 52, Printed circuits, was submitted to the IEC-CENELEC parallel vote and was approved by CENELEC as EN 62326-4-1 on 1996-12-09.

The following dates were fixed:

- latest date by which the EN has to be implemented at national level by publication of an identical national standard or by endorsement (dop) 1997-09-01
- latest date by which the national standards conflicting with the EN have to be withdrawn (dow) -

This section 1 of part 4 is to be used in conjunction with EN 62326-1:1997 and EN 62326-4:1997

Annexes designated "normative" are part of the body of the standard.
Annexes designated "informative" are given for information only.
In this standard, annex ZA is normative and annexes A, B and C are informative.
Annex ZA has been added by CENELEC.

Endorsement notice

The text of the International Standard IEC 2326-4-1:1996 was approved by CENELEC as a European Standard without any modification.

Annex ZA (normative)

Normative references to international publications with their corresponding European publications

This European Standard incorporates by dated or undated reference, provisions from other publications. These normative references are cited at the appropriate places in the text and the publications are listed hereafter. For dated references, subsequent amendments to or revisions of any of these publications apply to this European Standard only when incorporated in it by amendment or revision. For undated references the latest edition of the publication referred to applies (including amendments).

NOTE: When an international publication has been modified by common modifications, indicated by (mod), the relevant EN/HD applies.

Publication	Year	Title	EN/HD	Year
IEC 68-2-3	1969	Basic environmental testing procedures Part 2: Tests - Test Ca: Damp heat, steady state	HD 323.2.3 S2[1)]	1987
IEC 68-2-20	1979	Test T: Soldering	HD 323.2.20 S3[2)]	1988
IEC 68-2-38	1974	Test Z/AD: Composite temperature/humidity cyclic test	HD 323.2.38 S1	1988
IEC 249-3-3	1991	Base materials for printed circuits Part 3: Special materials used in connection with printed circuits Specification No. 3: Permanent polymer coating materials (solder resist) for use in the fabrication of printed boards	-	-
IEC 1189-3	[3)]	Test methods for electrical materials, interconnection structures and assemblies Part 3: Test methods for interconnection structures (printed boards)	-	-
IEC 2326-1	1996	Printed boards Part 1: Generic specification	EN 62326-1	1997
IEC 2326-4	1996	Part 4: Rigid multilayer printed boards with interlayer connections Sectional specification	EN 62326-4	1997

1) HD 323.2.3 S2 includes A1:1984 to IEC 68-2-3.

2) HD 323.2.20 S3 includes A2:1987 to IEC 68-2-20.

3) At present under IEC-CENELEC parallel vote (52/627/FDIS).

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Cartes imprimées –

Partie 4:
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Printed boards –

Part 4:
Rigid multilayer printed boards with interlayer connections – Sectional specification – Section 1: Capability Detail Specification – Performance levels A, B and C

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Международная Электротехническая Комиссия

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Pour prix, voir catalogue en vigueur
For price, see current catalogue

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

PRINTED BOARDS –

Part 4: Rigid multilayer printed boards with interlayer connections – Sectional specification – Section 1: Capability Detail Specification – Performance levels A, B and C

FOREWORD

1) The IEC (International Electrotechnical Commission) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of the IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, the IEC publishes International Standards. Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. The IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.

2) The formal decisions or agreements of the IEC on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested National Committees.

3) The documents produced have the form of recommendations for international use and are published in the form of standards, technical reports or guides and they are accepted by the National Committees in that sense.

4) In order to promote international unification, IEC National Committees undertake to apply IEC International Standards transparently to the maximum extent possible in their national and regional standards. Any divergence between the IEC Standard and the corresponding national or regional standard shall be clearly indicated in the latter.

5) The IEC provides no marking procedure to indicate its approval and cannot be rendered responsible for any equipment declared to be in conformity with one of its standards.

6) Attention is drawn to the possibility that some of the elements of this International Standard may be the subject of patent rights. The IEC shall not be held responsible for identifying any or all such patent rights.

International Standard IEC 2326-4-1 has been prepared by IEC technical committee 52: Printed circuits.

This standard cancels and replaces IEC 326-6.

This standard should be read in conjunction with IEC 2326-1 and IEC 2326-4

The text of this standard is based on the following documents:

DIS	Report on voting
52/656/DIS	52/678/RVD

Full information on the voting for approval of this standard can be found in the report on voting indicated in the above table.

Annexes A, B and C are for information only.

The QC number that appears on the front cover of this publication is the specification number in the IEC Quality Assessment System for Electronic Components (IECQ).

PRINTED BOARDS –

Part 4: Rigid multilayer printed boards with interlayer connection – Sectional specification – Section 1: Capability Detail Specification – Performance levels A, B and C

1 Scope

This Capability Detail Specification (Cap DS) is based on IEC 2326-4. It relates to rigid multilayer printed boards with interlayer connections manufactured with materials specified in 3.1. It specifies the capability qualifying component (CQC), the characteristics to be tested, the test methods and conditions to be applied and the requirements to be fulfilled for testing capability for performance level A, B or C.

2 Normative references

The following normative documents contain provisions which, through reference in this text, constitute provisions of IEC 2326-4. At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on this section of IEC 2326-4 are encouraged to investigate the possibility of applying the most recent editions of the standards indicated below. Members of IEC and ISO maintain registers of currently valid International Standards.

IEC 68-2-3: 1969, *Environmental testing – Part 2: Tests – Test Ca: Damp heat, steady state*

IEC 68-2-20: 1979, *Environmental testing – Part 2: Tests – Test T: Soldering*

IEC 68-2-38: 1974, *Environmental testing – Part 2: Tests – Test Z/AD: Composite temperature/humidity cyclic test*

IEC 249-3-3: 1991, *Base materials for printed circuits – Part 3: Special materials used in connection with printed circuits – Specification No. 3: Permanent polymer coating materials (solder resist) for use in the fabrication of printed boards*

IEC/FDIS 1189-3: *Test methods for electrical materials, interconnection structures and assemblies – Part 3: Test methods for interconnection structures*[1)]

IEC 2326-1: 1996, *Printed boards – Part 1: Generic specification*

IEC 2326-4: 1996, *Printed boards – Part 4: Rigid multilayer printed boards with interlayer connections – Sectional specifications*

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1) At present at the stage of Final Draft International Standard.

3 Capability Qualifying Component (CQC)

Test specimens to be used as CQCs are described in clause 6 and shall:

- be made of one of the copper clad base materials and one of the bonding sheet materials specified in 3.1;
- have a construction that has one set of characteristics identified in table 2;
- bear the required portions of the capability test board specified in 6.1; as an alternative a production panel may be used. Portions of the production panel may be used as test specimens provided that they are similar to those shown in figure 1.

3.1 *Materials*

Table 1 – Materials

Material group code	Base material	
	IEC	Type
M1	1249-2-7 1249-4-1	Part 2: Sectional specification set for reinforced base materials, clad and unclad - Section 7: Epoxide woven glass laminate Part 4: Sectional specification set for prepreg materials, unclad - Section 1: Epoxide woven glass prepregs
M2	1249-2-11 1249-4-1	Part 2: Sectional specification set for reinforced base materials, clad and unclad - Section 11: Polyimide woven glass laminate Part 4: Sectional specification set for prepreg materials, unclad - Section 1: Epoxide woven glass prepregs
M3	1249-2-9 1249-4-1	Part 2: Sectional specification set for reinforced base materials, clad and unclad - Section 9: Bismaleimide/Triazine modified epoxide woven glass laminate Part 4: Sectional specification set for prepreg materials, unclad - Section 1: Epoxide woven glass prepregs

3.2 *Product capability*

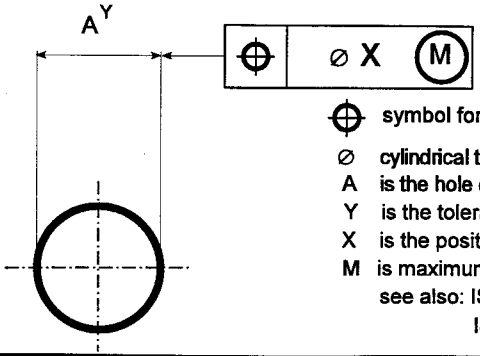
The individual test specimens (ITS) containing the CQC for capability testing shall represent the grade of capability. This grade may be described by an alphanumeric codification developed from table 2. To each codification letter from table 2 representing three or one properties (three for the characteristics A, B, C, D and one for E) belong three or one of the figures (digit) 1 to 9 representing the grade of the relevant property. The sequence of these figures corresponds to the sequence of the properties stated in table 2. For example: A356B435C456D334E6.

Table 2 – Product capability

Criteria				Code indication	1	2	3	4	5	6	7	8	9
BOARD	Board size (diagonal)		mm	A	≤150	250	350	450	550	650	750	850	>850
	Total board thickness		mm		≤0,5	1,0	1,6	2,0	2,5	3,5	5,0	6,5	>6,5
	Number of conductive layers		--		3-4	5-6	7-8	9-12	13-16	17-20	21-24	25-28	>28
HOLES	Diameter of as-drilled holes		mm	B	≥0,6	0,5	0,4	0,35	0,30	0,25	0,20	0,15	<0,15
	Total tolerance of drilled hole (min.-max.)		mm		≥0,300	0,250	0,200	0,150	0,125	0,100	0,075	0,050	<0,050
	Location of hole. Positional tolerance **		mm		≥0,60	0,50	0,40	0,30	0,25	0,20	0,15	0,10	<0,10
CONDUCTORS *	Unplated (inner) layers	Minimum electrical clearance	mm	C	≥0,500	0,350	0,250	0,200	0,150	0,125	0,100	0,075	<0,075
		Minimum conductor width	mm		≥0,300	0,250	0,200	0,150	0,125	0,100	0,075	0,050	<0,050
		Conductor process allowance (min.-max.)	mm		≥0,150	0,100	0,075	0,050	0,040	0,030	0,025	0,020	<0,020
	Plated (outer layers)	Minimum electrical clearance	mm	D	≥0,500	0,350	0,250	0,200	0,150	0,125	0,100	0,075	<0,075
		Minimum conductor width	mm		≥0,300	0,250	0,200	0,150	0,125	0,100	0,075	0,050	<0,050
		Conductor process allowance (min.-max.)	mm		≥0,150	0,100	0,075	0,050	0,040	0,030	0,025	0,020	<0,020
POSITIONAL	Location of features (conductive and non-conductive pattern) Positional tolerance **		mm	E	≥0,60	0,50	0,40	0,30	0,25	0,20	0,15	0,10	<0,10

* The grid (or pitch) can be calculated as follows:
minimum electrical clearance + conductor process allowance + minimum conductor width

** Positional tolerance:



⊕ symbol for position
⌀ cylindrical tolerance zone
A is the hole diameter
Y is the tolerance of the hole
X is the positional tolerance of the hole
M is maximum material principle
see also: ISO 2692
ISO 5458

3.3 *Process capability*

The CQC shall be produced with one or more of the processes given in table 3. The descriptions of the processes given in table 3 identify the total processes used in the facility to produce printed board products. These processes include toolings and primary imagings (W), plating processes (X), coatings (Y) and testing (Z).

Not all processes need to be used on a single product CQC; however, to obtain process capability approval all processes claimed must be available for review.

Table 3 – Tooling and processes

Code indication	W Toolings and primary imagings			X Plating processes				Y Coatings			Z Testing
	Photo tooling	Electronic data	Image transfer	Initial plated holes	Conductive	Standard overplate	Precious overplate	Metallic	Permanent polymer	Organic	
1	Glass image reduction and manipulation (photographic)	CAD data acceptance (electrical)	Screen imaging	Electroless initial through-hole interconnection	Electrolytic copper plating	Tin-lead plating	Gold and gold on nickel (contact areas)	Solder (roller coated)	Dry film permanent polymer coating	Copper conservation coating flux	Electrical continuity tests
2	Film image reduction and manipulation (photographic)	CAD data and CAM (electrical)	Photoimaging	Conductive coatings for initial through-hole interconnection	Semi-additive	Tin plating	Bond gold plating	Solder (hot levelled, air or oil)	Liquid permanent polymer coating (photodefined)	Conformal coating	Optical inspection
4	Photo tool generation (plotter)	Other image tool	Direct imaging	Other processes for initial through-hole interconnection	Electroless copper plating (additive)	Other standard platings	Other exotic platings	Other solder applications	Liquid permanent polymer coating (screened)	Other organic coatings	Other testing

The codification of the process capability shall be developed from table 3. The process code is a series of significant letters (W, X, Y and Z, each corresponding to a group of processes), each followed by one, three or four figures representing the columns within the group of processes. According to table 3 the figures are 1, 2 or 4. If the manufacturer uses none, two or three of the referred facilities within a column, the following figure shall be used:

0 = no capability approval for that particular process of W, X, Y or Z
1 = only 1
2 = only 2
3 = 1 and 2
4 = only 4

5 = 1 and 4
6 = 2 and 4
7 = 1, 2 and 4

Example: The code W416X2732Y150Z3 is used when a manufacturer has claimed the following facilities:

Tooling (W)	4 (first column) :	Photo tool generation (plotter)
	1 (second column) :	CAD data acceptance (electronic)
	6 (third column) :	Photo imaging and direct imaging
Plating processes (X)	2 (first column) :	Conductive coatings for initial through-hole interconnection
	7 (second column) :	Electrolytic copper plating, electrolysis copper plating (additive) and semi-additive
	3 (third column) :	Tin-lead plating and tin plating
	2 (fourth column) :	Bond gold plating
Coatings (Y)	1 (first column) :	Solder (roller coated)
	5 (second column) :	Dry film permanent polymer coating and liquid permanent polymer coating (screened)
	0 (third column) :	*No* capability approval for organic coatings
Testing (Z)	3 (first column) :	Electrical continuity tests and optical inspection

4 Capability approval

4.1 *Range of capability approval*

Capability approval granted on testing one product combination within the limits specified in 5.7 of IEC 2326-1 and the following:

- base materials according to 3.1;
- the maximum product characteristics according to 3.2;
- processes used according to 3.3.

4.2 *Qualified Manufacturers List (QML) information*

The QML information shall be given in accordance with 5.4 of IEC 2326-1 and shall contain the following details related to this Cap DS:

- reference to this Cap DS: 2326-4-1;
- description of features for which capability approval is granted:
  - identify the material in accordance with table 1;
  - identify the product in accordance with table 2;
  - identify the processes in accordance with table 3.

For example: 2326-4-1B/M1A356B435C456D334E6W416X2732Y150Z3

Remark:
This code description is used by a computer system to establish a product type made by a manufacturer. The code facilitates using (a) computer system(s) to categorize manufacturers, to help in sorting products listing by a specific product characteristic, or to provide ease of matching a users' product requirement with a manufacturers' capability. When this code is used in conjunction with a QPL or QML the manufacturer has the capability to make:

(2326-4-1) – a rigid multilayer printed board with interlayer connections;
(B) – of level B performance (covers both levels A and B);
(M1) – this board is made of base materials according to IEC 1249-2-7 and IEC 1249-4-1.

The board has the following characteristics:

(A356) maximum board size of 350 mm diagonal;
maximum total board thickness of 2,5 mm;
maximum number of conductive layers of 20;
(B435) smallest diameter of as-drilled holes of 0,35 mm;
smallest total tolerance of drilled hole of 0,200 mm;
smallest location of hole (diameter from true position) of 0,25 mm;
(C456) smallest electrical clearance (inner layer) of 0,200 mm;
smallest minimum conductor width (inner layer) of 0,125 mm;
smallest total required manufacturing allowance (inner layer) of 0,030 mm;
(D334) smallest electrical clearance (outer layer) of 0,250 mm;
smallest minimum conductor width (outer layer) of 0,200 mm;
smallest total required manufacturing allowance (outer layer) of 0,050 mm;
(E6) smallest location of features (diameter from true position) of 0,20 mm.

The toolings and processes available are:

(W416) photo tool generation (plotter);
CAD data acceptance (electrical);
photo and direct imaging;
(X2732) conductive coatings for initial through-hole interconnection;
electrolytic copper plating, electrolysis copper plating (additive) and semi-additive plating;
tin-lead and tin platings;
bond gold plating;
(Y150) solder (roller coated);
dry film permanent polymer coating and liquid permanent polymer coating (screened);
(Z3) electrical continuity tests and optical inspection.

5 Capability testing

5.1 *Capability test programme*

The capability test programme, the number of specimens to be tested shall be applied as specified in table 4.

The test sequence is given in clause 6 of IEC 2326-4.

5.2 *Characteristics*

The characteristics given in table 4 shall be tested. The test methods and conditions given there for the appropriate performance level shall be applied and the requirements given there shall be fulfilled.
No defects are allowed.