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Omreǵni vidiki (NA) ï Velemestno omreǵje (MAN) ï Konvergenļ ni postopek na fiziļ ni plasti za hitrost 155,520 Mbit/s

Network Aspects (NA); Metropolitan Area Network (MAN); Physical layer convergence procedure for 155,520 Mbit/s

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Foreword

This European Telecommunication Standard (ETS) has been prepared by the Network Aspects (NA) Technical Committee of the European Telecommunications Standards Institute (ETSI).

This ETS details the physical layer convergence procedure for a European Metropolitan Area Network (MAN) based on the Distributed Queue Dual Bus (DQDB) access method as defined in IEEE Standard 802.6 [6] operating at a transmission rate of 155,520 Mbit/s in accordance with CCITT Recommendations G.707 [1], G.708 [2] and G.709 [3].

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1 Scope

This European Telecommunication Standard (ETS) defines the physical layer convergence procedure at 155,520 Mbit/s for use in the context of a subnetwork of a Metropolitan Area Network (MAN). Use of methods defined in this ETS for other purposes is outside the scope of this ETS.

Methods of testing will be the subject of separate arrangements.

2 Normative references

This ETS incorporates, by dated or undated reference, provisions from other publications. These normative references are cited at the appropriate places in the text and the publications are listed hereafter. For dated references, subsequent amendments to, or revisions of any of these publications apply to this ETS only when incorporated in it by amendment or revision. For undated references the latest edition of the publication referred to applies.

[1] CCITT Recommendation G.707 (1991): "Synchronous digital hierarchy bit rates".

[2] CCITT Recommendation G.708 (1991): "Network node interface for the synchronous digital hierarchy".

[3] CCITT Recommendation G.709 (1991): "Synchronous multiplexing structure".

[4] CCITT Recommendation G.783 (1991): "Characteristics of synchronous digital hierarchy (SDH) multiplexing equipment functional blocks".

[5] CCITT Recommendation I.432 (1991): "B-ISDN user-network interface - Physical layer specification".

[6] IEEE Standard 802.6 (1990): "Distributed Queue Dual Bus (DQDB) Subnetwork of a Metropolitan Area Network (MAN)".

3 Definitions

For the purposes of this ETS, the definitions as defined in IEEE Standard 802.6 [6] apply.

4 Symbols and abbreviations

For the purposes of this ETS, the symbols and abbreviations as defined in IEEE Standard 802.6 [6] apply.

5 Physical Layer Convergence Procedure (PLCP) for 155,520 Mbit/s CCITT Recommendations G.707, G.708, G.709 SDH based systems

5.1 Introduction

This ETS defines a convergence procedure for transfer of Distributed Queue Dual Bus (DQDB) slots using the Synchronous Digital Hierarchy (SDH) at a 155,520 Mbit/s physical medium rate. The rates, formats, and other attributes of SDH are defined in CCITT Recommendations G.707 [1], G.708 [2] and G.709 [3]. DQDB slots are mapped into VC-4 virtual containers, and the VC-4s are transported using synchronous transport modules. A mapping of Asynchronous Transfer Mode (ATM) cells into VC-4 can be found in CCITT Recommendation I.432 [5]. As ATM cells and DQDB slots are identical in length (53 octets) and nearly identical in format, the mapping of DQDB slots into VC-4 is identical to the ATM cell mapping into VC-4 except for the following:

- the use of the user channel (F2) and growth (Z3) octets for carrying DQDB layer management information octets (M1 and M2);

- the use of two bit positions in the multiframe indicator (H4) octet for providing the DQDB Link Status Signal (LSS);

- the use of VC-4 for propagating the DQDB layer 125 µs timing along the DQDB buses;

- the optional use of either six bit positions in the multiframe indicator (H4), or the Header Check Sequence (HCS) method for providing slot boundary indication. The HCS method for slot delineation is identical to the Header Error Control (HEC) method for ATM cell delineation described in CCITT Recommendation I.432 [5], section 4.5.1.1, except for the fact that the HCS is calculated over three octets of the DQDB slot header, whereas the ATM HEC is calculated over four octets of the ATM cell header.

CCITT Recommendations G.707 [1], G.708 [2], and G.709 [3] shall be the primary references for providing an SDH based physical layer for DQDB with the above modifications. Descriptions of Path OverHead (POH) field definitions in this ETS other than (M1, M2) and H4 fields are included for clarity and completeness only.

The SDH PLCP makes use of the optional status parameter in Ph-DATA indication and Ph-DATA request primitives (see IEEE Standard 802.6 [6], section 4.2). Hence, the status parameter is mandatory for the service provided by the SDH PLCP.

In this ETS , the terms bus x, bus y, Ph-SAP_x, and Ph-SAP_y (x = A or B; y = B or A) will be used. Bus x enters a DQDB node at Ph-SAP_x and exits at Ph-SAP_y whereas bus y enters a DQDB node at Ph-SAP_y and exits at Ph-SAP_x.

5.2 The PLCP frame format

The PLCP frame format is a virtual container VC-4 that consists of 9 rows by 261 octets. The VC-4 has a nominal duration of 125 µs. The VC-4 frame rate shall provide the 125 µs timing information. The VC-4 frames are transported between peer PLCPs by the SDH transmission system.

DQDB slots are mapped into the VC-4 as illustrated in figure 1. The VC-4 consists of one column (nine octets) of POH plus a 9 row by 260 column payload capacity.

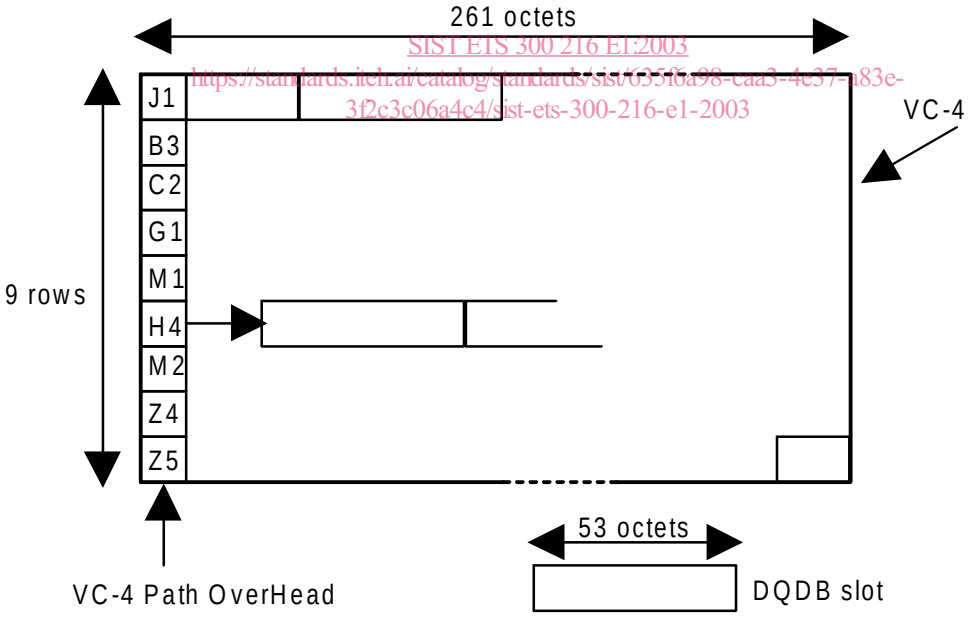

Figure 1: VC-4 PLCP mapping for DQDB

The DQDB slots are located horizontally (by row) in the VC-4 payload capacity with the slot boundaries aligned with the VC-4 octet boundaries. Because the VC-4 payload capacity (2 340 octets) is not an integer multiple of the DQDB slot length (53 octets), a slot is allowed to cross the VC-4 boundary. Slot boundary indication shall be provided on a 125 µs basis by use of the POH H4 octet.

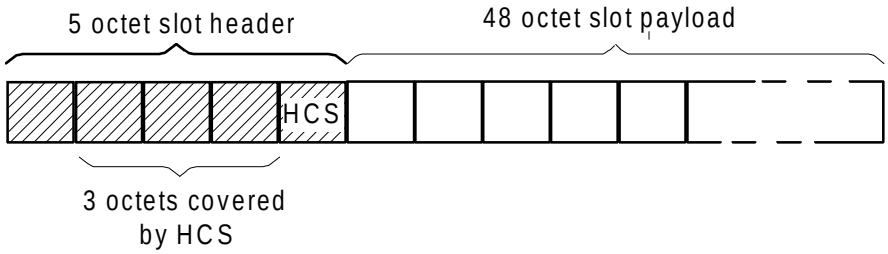

Figure 2: DQDB slot format

The slot format is illustrated in figure 2. The slot payload of 48 octets shall be scrambled before VC-4 framing. The scrambler operates for the duration of the 48 octet slot payload. Operation is suspended and the scrambler state is retained at all other times. A self-synchronous scrambler with generator polynomial $x^{43}+1$ shall be used. In the reverse operation, following termination of the VC-4 signal and slot delineation, the slot payload shall be de-scrambled. The de-scrambler operates for the duration of the assumed slot payload according to the derived slot delineation (see subclause 5.6.1.1). Operation is suspended and the de-scrambler state is retained at all other times.

At the transmitting PLCP, an eight bit pattern shall be added (modulo 2) to the HCS field of the slot headers. At the receiving PLCP, the same bit pattern shall be subtracted (equal to add modulo 2) from the HCS field of the assumed slot headers. The bit pattern shall be (01010101).

5.3 PLCP path overhead field definitions

The first column of the VC-4 contains the path overhead octets. The following subclauses describe each of the VC-4 path overhead octets and their functions. As previously noted, these descriptions are consistent with CCITT Recommendation G.709 [3] except for the use of the user channel (F2), growth (Z3), and multiframe indicator (H4) octets. Values of octets are described as bit patterns. The leftmost bit of each octet is most significant.

The PLCP path is defined between two adjacent peer PLCP entities. All path overhead octets other than M1 and M2 are related to PLCP operation and are terminated/generated at each PLCP on the subnetwork. The M1 and M2 octets are provided for the transport of DQDB layer management information octets and shall not be processed by the PLCP.

5.3.1 Path trace (J1)

The J1 octet is used to repetitively transmit a 64 octet, fixed length string so that a receiving PLCP can verify its continued connection to the intended transmitter PLCP.

5.3.2 Bit Interleaved Parity - 8 (B3)

The B3 octet is allocated for the PLCP path error monitoring function. This function shall be a Bit Interleaved Parity-8 (BIP-8) code using even parity. The PLCP path BIP-8 is calculated over all bits of the previous VC-4. The computed BIP-8 is placed in the B3 octet of the current VC-4. The BIP-8 is calculated after the PLCP scrambling of the slot payload.

A BIP-8 is an 8 bit code in which the first bit of the BIP-8 code calculates even parity over the first bit of each octet in the VC-4, the second bit of the BIP-8 code calculates even parity over the second bit of each octet in the VC-4, etc. Therefore, the BIP-8 code provides for 8 separate even parity codes covering the corresponding bit of each octet in the VC-4.