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Omreǵni vidiki (NA) ï Velemestno omreǵje (MAN) ï Konvergenļ ni postopek na fiziļ ni plasti (PLCP) za hitrost 622,080 Mbit/s ï Priporoļ ila CCITT G.707, G.708 in G.709 ï Na SDH temeljeļ i sistemi

Network Aspects (NA); Metropolitan Area Network (MAN); Physical Layer Convergence Procedure (PLCP) for 622,080 Mbit/s CCITT Recommendations G.707, G.708 and G.709 SDH based systems

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Foreword

This European Telecommunication Standard (ETS) has been prepared by the Network Aspects (NA) Technical Committee of the European Telecommunications Standards Institute (ETSI).

This ETS details the physical layer convergence procedure for a European Metropolitan Area Network (MAN) based on the Distributed Queue Dual Bus (DQDB) access method as defined in IEEE Standard 802.6 [6] operating at a transmission rate of 622,080 Mbit/s in accordance with CCITT Recommendations G.707 [1], G.708 [2] and G.709 [3].

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1 Scope

This European Telecommunication Standard (ETS) defines the physical layer convergence procedure at 622,080 Mbit/s for use in the context of a subnetwork of a Metropolitan Area Network (MAN). Use of methods defined in this ETS for other purposes is outside the scope of this ETS.

Methods of testing will be the subject of separate arrangements.

2 Normative references

This ETS incorporates, by dated or undated reference, provisions from other publications. These normative references are cited at the appropriate places in the text and the publications are listed below. For dated references, subsequent amendments to or revisions of these publications apply to this ETS only when incorporated in it by amendment or revision. For undated references the latest edition of the publication referred to applies.

[1] CCITT Recommendation G.707 (1991): "Synchronous Digital Hierarchy Bit Rates".

[2] CCITT Recommendation G.708 (1991): "Network Node Interface for the Synchronous Digital Hierarchy".

[3] CCITT Recommendation G.709 (1991): "Synchronous Multiplexing Structure".

[4] CCITT Recommendation G.783 (1991): "Characteristics of Synchronous Digital Hierarchy (SDH) Multiplexing Equipment Functional Blocks".

[5] CCITT Recommendation I.432 (1991): "B-ISDN User-Network Interface - Physical Layer Specification".

[6] IEEE Standard 802.6 (1990): "Distributed Queue Dual Bus (DQDB) Subnetwork of a Metropolitan Area Network (MAN)".

[7] ETS 300 147: "Transmission and multiplexing; Synchronous digital hierarchy multiplexing structure".

3 Definitions

For the purpose of this ETS, the definitions as defined in IEEE Standard 802.6 [6] shall apply.

4 Symbols and abbreviations

For the purpose of this ETS, the symbols and abbreviations as defined in IEEE Standard 802.6 [6] shall apply.

5 Physical layer convergence procedure for 622,080 Mbit/s CCITT Recommendations G.707, G.708 and G.709 SDH based systems

5.1 Introduction

This ETS defines a convergence procedure for transfer of Distributed Queue Dual Bus (DQDB) slots using the Synchronous Digital Hierarchy (SDH) at a 622,080 Mbit/s physical medium rate.

The rates, formats, and other attributes of SDH are defined in CCITT Recommendations G.707 [1], G.708 [2] and G.709 [3]. DQDB slots are mapped into VC-4-4c virtual containers, and the VC-4-4c's are transported using synchronous transport modules. A mapping of Asynchronous Transfer Mode (ATM) cells into VC-4-4c can be found in CCITT Recommendation I.432 [5]. As ATM cells and DQDB slots are identical in length (53 octets) and nearly identical in format, the mapping of DQDB slots into VC-4-4c is identical to the ATM cell mapping into VC-4-4c except for the following:

- the use of the user channel (F2) and growth (Z3) octets for carrying DQDB layer management information octets (M1 and M2);

- the use of two bit positions in the multiframe indicator (H4) octet for providing the DQDB Link Status Signal (LSS);

- the use of VC-4-4c for propagating the DQDB layer 125 µs timing along the DQDB buses;

- the Header Check Sequence (HCS) method shall be used for providing slot boundary indication. The HCS method for slot delineation is identical to the Header Error Control (HEC) method for ATM cell delineation described in CCITT Recommendation I.432 [5], § 4.5.1.1 except for the fact that the HCS is calculated over three octets of the DQDB slot header, whereas the ATM HEC is calculated over four octets of the ATM cell header.

CCITT Recommendations G.707 [1], G.708 [2] and G.709 [3] shall be the primary references for providing an SDH based physical layer for DQDB with the above modifications. Descriptions of POH field definitions in this ETS other than M1-M2 and H4 fields are included for clarity and completeness only.

The SDH PLCP makes use of the optional status parameter in Ph-DATA indication and Ph-DATA request primitives (see section 4.2 of IEEE Standard 802.6 [6]). Hence, the status parameter shall be mandatory for the service provided by the SDH PLCP.

In this ETS, the terms Bus x, Bus y, Ph-SAP_x, and Ph-SAP_y (x = A or B; y = B or A) are used. Bus x enters a DQDB node at Ph-SAP_x and exits at Ph-SAP_y, whereas Bus y enters a DQDB node at Ph-SAP_y and exits at Ph-SAP_x.

5.2 The PLCP frame format

The PLCP frame format is a virtual container VC-4-4c that consists of 9 rows by 1 044 octets. The VC-4-4c has a nominal duration of 125 µs. The VC-4-4c frame rate shall provide the 125 µs timing information. The VC-4-4c frames are transported between peer PLCPs by the SDH transmission system.

DQDB slots are mapped into the VC-4-4c as illustrated in figure 1. The VC-4-4c consists of one column (nine octets) of Path Overhead (POH), three columns of unused octets plus a 9 row by 1 040 column payload capacity.

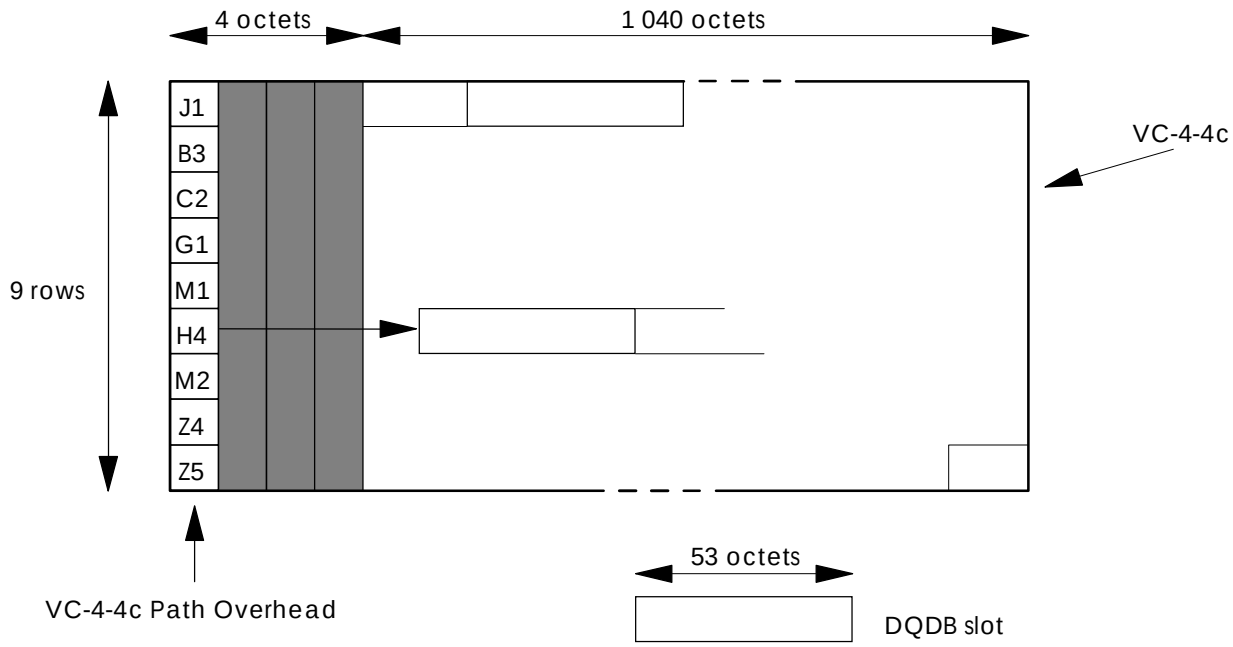

Figure 1: VC-4-4c PLCP mapping for DQDB

The DQDB slots are located horizontally (by row) in the VC-4-4c payload capacity with the slot boundaries aligned with the VC-4-4c octet boundaries. Because the VC-4-4c payload capacity (9 360 octets) is not an integer multiple of the DQDB slot length (53 octets), a slot is allowed to cross the VC-4-4c boundary. Slot boundary indication shall be provided using the HCS method.

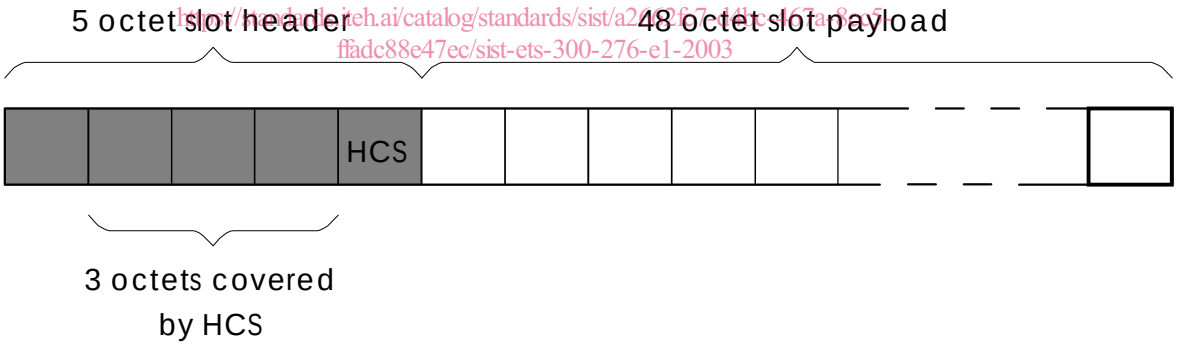

Figure 2: DQDB slot format

The slot format is illustrated in figure 2. The slot payload of 48 octets shall be scrambled before VC-4-4c framing. The scrambler operates for the duration of the 48 octet slot payload. Operation is suspended and the scrambler state is retained at all other times. A self-synchronous scrambler with generator polynomial $x^{43}+1$ shall be used. In the reverse operation, following termination of the VC-4-4c signal and slot delineation, the slot payload shall be descrambled. The descrambler shall operate for the duration of the assumed slot payload according to the derived slot delineation (see subclause 5.6.1.1). Operation shall be suspended and the descrambler state shall be retained at all other times.

At the transmitting PLCP, an eight bit pattern shall be added (modulo 2) to the HCS field of the slot headers. At the receiving PLCP, the same bit pattern shall be subtracted (equal to add modulo 2) from the HCS field of the assumed slot headers. The bit pattern shall be (01010101).