Designation: E431 – 96(Reapproved 2011)

Standard Guide to Interpretation of Radiographs of Semiconductors and Related Devices[1]

This standard is issued under the fixed designation E431; the number immediately following the designation indicates the year of original adoption or, in the case of revision, the year of last revision. A number in parentheses indicates the year of last reapproval. A superscript epsilon (ε) indicates an editorial change since the last revision or reapproval.

1. Scope

1.1 This guide provides illustrations of radiographs of semiconductors and related devices. Low powered transistors (through the TO-11 case configuration), diodes, low-power rectifiers, power devices, and integrated circuits are illustrated with common assembly features. Particular areas of construction are featured for these devices detailing critical points of design or assembly.

1.2 *This standard does not purport to address all of the safety concerns, if any, associated with its use. It is the responsibility of the user of this standard to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use.*

2. Referenced Documents

2.1 *ASTM Standards:*[2]

E801 Practice for Controlling Quality of Radiological Examination of Electronic Devices

E1161 Practice for Radiologic Examination of Semiconductors and Electronic Components

E1255 Practice for Radioscopy

E1316 Terminology for Nondestructive Examinations

3. Terminology

3.1 Definitions of terms used in these reference illustrations may be found in Terminology E1316, Section D.

4. Significance and Use

4.1 Illustrations provided in this guide are intended for use as references to aid in interpreting film or nonfilm images resulting from x-ray examinations (see Table 1) to ascertain quality of assembly and workmanship.

4.2 Required attributes of the design features or other construction details are not provided but are to be established as mutually agreed upon by manufacturers and users of these devices. Many devices share common assembly features; thus, these interpretations can be used for components not illustrated.

5. Use of Illustrations

5.1 The illustrations in this guide are for use in interpreting radiographs of semiconductors and related devices. They provide reference points and information on the critical areas of such devices. These points must be clearly resolved in the radiographs being interpreted. The radiographs to be interpreted must comply with the requirements of Practice E801 to ensure suitable image quality with minimal distortion. Additional information on the application of radiographic techniques to semiconductors and electronic components may be found in Test Method E1161.

5.2 The illustrations in this guide may also be used to interpret the radioscopic images of semiconductors and related devices when using radioscopic techniques. The radioscopic images to be interpreted must comply with the requirements of Practice E801 to ensure suitable image quality with minimal distortion. Additional information on the application of radioscopic techniques may be found in Test Method E1161 and Practice E1255.

6. Description

6.1 Description of irregularities and applicable figures are shown in Table 1.

[1] This guide is under the jurisdiction of ASTM Committee E07 on Nondestructive Testing and is the direct responsibility of Subcommittee E07.02 on Reference Radiological Images.

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[2] For referenced ASTM standards, visit the ASTM website, www.astm.org, or contact ASTM Customer Service at service@astm.org. For *Annual Book of ASTM Standards* volume information, refer to the standard's Document Summary page on the ASTM website.

7. Keywords

7.1 electronic devices; nondestructive testing; radiographs; radiography; reference illustrations; semiconductors; x-ray

TABLE 1 Irregularity Description and Figure References

Item and Irregularity	Expressed as	Figure Reference
	Transistors, low-power (TO-11 and smaller packages)	
Extraneous matter	Any material contained in the semiconductor device that is not necessary for its manufacture or operation.	1
Internal lead irregularities, bond-to-post connection	Leads extending beyond attachment points at either end. Allowable extension should be stated in wire diameters.	2(*a*)
	Slack leads deviate from a straight line between attachment points. Allowable deviation should be stated in wire diameters.	2(*b*)
	Internal lead clearance is the distance between the edge of the chip and lead wire. Allowable clearance should be stated in wire diameters.	2(*c*)
Post-position irregularities	Allowable deviations of the post from its intended (design) position may be specified as minimum angle made by the post and header, or as clearance between post and post or post and case expressed in terms of post diameter.	3
Getter-position irregularities	In crimp-type devices, deviations of the getter ring from its intended (design) position are stated relative to the crimp. In noncrimp-type devices, deviations of the getter ring from its intended (design) position are stated as the angle between the actual and intended positions.	4(*a*) 4(*b*)
Mounting paste	Mounting-paste buildup or expulsion, or both, is an excessive amount of material used to mount the semiconductor element on the header. Allowable excess should be measured relative to the surfaces, clearances, and shape of the deposit.	5
Post-connection solder or gold paste	Post-connection solder or gold-paste buildup is an excessive amount of such material at the termination. Excess is measured relative to the diameter at the attachment point and by the deposit shape.	6
	Diodes and low-power rectifiers (whisker-type)	
Extraneous matter	Any material contained in the cavity of the device that is not part of its design and not required for its manufacture or operation.	7(*a*) 7(*b*) 7(*c*)
Whisker irregularities	Any whisker malformation from its intended shape caused by compression. Allowable compression is stated as a percentage of design length.	8(*a*)
	Whisker cross-sectional—area deviations are stated as a percentage of cross section.	8(*b*)
	Misalignment irregularities are described by device design and type of construction.	none
	Whisker contact to the post or lead is expressed as a percentage of the design contact area.	8(*c*)
Crimped lead devices	Minimum crimp length can be stated.	9
Crystal and crystal-mounting irregularities	Tilt is the deviation of the mounted crystal from its intended (design) mounting plane. Allowable deviation is expressed in degrees from normal to the main axis of the device.	10(*a*)
	Clearance is the distance from the edge of the crystal to the inside wall of the device cavity. It is expressed in units of length (millimetres or inches); if contact is permissible, it should be stated whether or not fusion is allowable.	10(*b*) 10(*c*)
	Crystal fusion to the mount is an area of contact between the crystal and the designed mounting surface where fusion occurs. Minimum allowable fusion is stated as a percentage of the design mounting surface.	10(*d*)
	Mounting-paste expulsion is excessive mounting paste. Allowable expulsion is stated as deposit shape.	10(*e*)
	Diodes and low-power rectifiers (whiskerless-type)	
Misalignment	Crystal position relative to the posts or the posts to one another or both. Allowable crystal misalignment is stated as a percentage of the largest post. Allowable post misalignment is expressed as a percentage of the diameter of the smallest post.	11(*a*) 11(*b*)
Voids	Air bubbles in the encapsulation material used for the semiconductor device. Allowable voids are stated as a percentage of wall thickness and as the distance from the encapsulation ends to the lead seal.	12
	Integrated circuits	
Extraneous matter	Any material contained in the integrated circuit that is not part of its design and not necessary for its manufacture or operation.	none
Clearances	Minimum allowable clearances are expressed in units of length (millimetres or inches) or lead-wire diameters. Internal clearances can be stated between parts as: (*1*) lead to case; (*2*) lead wire to lead wire; (*3*) lead wire to bond; (*4*) lead wire to chip; (*5*) chip to chip; (*6*) bond to bond; (*7*) lead wire to external lead.	13
Chip mounting	The minimum area of mounting paste used to secure the chip to the header is stated as a percentage of the design contact (chip) area.	14(*a*)
	Unacceptable configuration of voids should be described.	14(*b*)
	A misaligned chip is one misoriented with respect to its intended position. Misalignment is expressed as an angle or a case-to-chip distance.	none
Mounting-paste buildup or expulsion (or both)	An excessive amount of the material used to mount the semiconductor element to the header. Allowable excess is measured relative to the top surface of the semiconductor element and by deposit shape.	5
Internal lead irregularities, bond-to-external lead, and bond-to-bond or bond-to-bond leads	Leads extending beyond the attachment points at either end. Allowable extension is stated in wire diameters.	none
	Slack leads deviate from a straight line between the attachment points. Allowable deviation is expressed in wire diameters.	none
	Power devices (transistors, rectifiers, and silicon-controlled rectifiers)	
Construction methods and designs	Because of the large variety of construction methods and designs, it will generally be necessary to state criteria for each type of device. The usual criteria should include examinations for: (*1*) extraneous matter; (*2*) internal clearances; (*3*) mounting-paste buildup and expulsion; (*4*) crimp irregularities, where internal leads are crimped into tubular, external leads; (*5*) internal-connection irregularities.	none

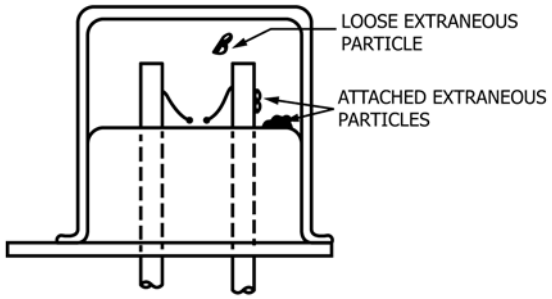
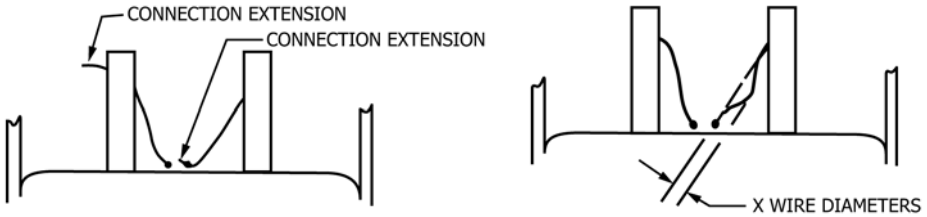
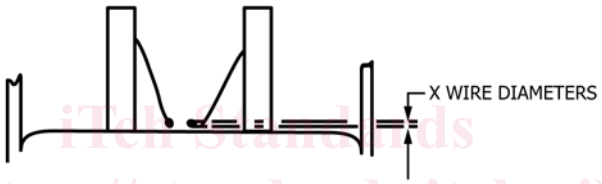


FIG. 1 Transistor—Extraneous Matter



(*a*) Bond-to-Post Connection

(*b*) Slack Leads



(*c*) Internal Lead Clearance

FIG. 2 Transistor—Internal Lead Irregularities

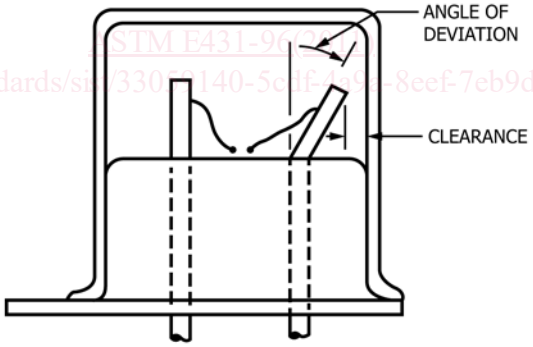


FIG. 3 Transistor—Post-Position Irregularities