SLOVENSKI STANDARD
oSIST prEN IEC 60749-26:2025

01-januar-2025

Polprevodniški elementi - Metode za mehansko in klimatsko preskušanje - 26. del: Preskušanje občutljivosti na elektrostatično razelektritev (ESD) - Model človeškega telesa (HBM)

Semiconductor devices - Mechanical and climatic test methods - Part 26: Electrostatic discharge (ESD) sensitivity testing - Human body model (HBM)

Halbleiterbauelemente - Mechanische und klimatische Prüfverfahren - Teil 26: Prüfung der Empfindlichkeit gegen elektrostatische Entladungen (ESD) - Human Body Model (HBM)

iTeh Standards
(https://standards.iteh.ai)
Document Preview

Dispositifs à semiconducteurs - Méthodes d'essais mécaniques et climatiques - Partie 26: Essai de sensibilité aux décharges électrostatiques (DES) - Modèle du corps humain (HBM)

oSIST prEN IEC 60749-26:2025
https://standards.iteh.ai/catalog/standards/sist/787de785-9b87-4f1a-b2dd-d3b61f47e4ad/osist-pren-iec-60749-26-2025

Ta slovenski standard je istoveten z: prEN IEC 60749-26:2024

ICS:

31.080.01	Polprevodniški elementi (naprave) na splošno	Semiconductor devices in general

oSIST prEN IEC 60749-26:2025 en

2003-01.Slovenski inštitut za standardizacijo. Razmnoževanje celote ali delov tega standarda ni dovoljeno.

iTeh Standards
(https://standards.iteh.ai)
Document Preview

oSIST prEN IEC 60749-26:2025
https://standards.iteh.ai/catalog/standards/sist/787de785-9b87-4f1a-b2dd-d3b61f47e4ad/osist-pren-iec-60749-26-2025

47/2882/CDV

COMMITTEE DRAFT FOR VOTE (CDV)

PROJECT NUMBER: **IEC 60749-26 ED5**	
DATE OF CIRCULATION: **2024-11-29**	CLOSING DATE FOR VOTING: **2025-02-21**
SUPERSEDES DOCUMENTS: **47/2872/RR**	

IEC TC 47 : SEMICONDUCTOR DEVICES	
SECRETARIAT: Korea, Republic of	SECRETARY: Mr Cheolung Cha
OF INTEREST TO THE FOLLOWING COMMITTEES:	HORIZONTAL FUNCTION(S):
ASPECTS CONCERNED:	
☒ SUBMITTED FOR CENELEC PARALLEL VOTING **Attention IEC-CENELEC parallel voting** The attention of IEC National Committees, members of CENELEC, is drawn to the fact that this Committee Draft for Vote (CDV) is submitted for parallel voting. The CENELEC members are invited to vote through the CENELEC online voting system.	☐ NOT SUBMITTED FOR CENELEC PARALLEL VOTING

iTeh Standards
(https://standards.iteh.ai)
Document Preview
oSIST prEN IEC 60749-26:2025
https://standards.iteh.ai/catalog/standards/sist/787de785-9b87-4f1a-b2dd-d3b61f47e4ad/osist-pren-iec-60749-26-2025

This document is still under study and subject to change. It should not be used for reference purposes.

Recipients of this document are invited to submit, with their comments, notification of any relevant patent rights of which they are aware and to provide supporting documentation.

Recipients of this document are invited to submit, with their comments, notification of any relevant "In Some Countries" clauses to be included should this proposal proceed. Recipients are reminded that the CDV stage is the final stage for submitting ISC clauses. (SEE AC/22/2007 OR NEW GUIDANCE DOC).

TITLE:

Semiconductor devices - Mechanical and climatic test methods - Part 26: Electrostatic discharge (ESD) sensitivity testing - Human body model (HBM)

PROPOSED STABILITY DATE: 2029

NOTE FROM TC/SC OFFICERS:

Copyright © 2024 International Electrotechnical Commission, IEC. All rights reserved. It is permitted to download this electronic file, to make a copy and to print out the content for the sole purpose of preparing National Committee positions. You may not copy or "mirror" the file or printed version of the document, or any part of it, for any other purpose without permission in writing from IEC.

oSIST prEN IEC 60749-26:2025

1 CONTENTS

2 FOREWORD 5
3 1. Scope 7
4 2. Normative references 7
5 3. Terms and definitions 7
6 4. Apparatus and required equipment 11
7 4.1. Waveform verification equipment 11
8 4.2. Oscilloscope 11
9 4.3. Additional requirements for digital oscilloscopes 12
10 4.4. Current probe 12
11 4.5. Evaluation loads 12
12 4.6. Attenuator 12
13 4.7. Human body model simulator 12
14 4.8. HBM test equipment parasitic properties 13
15 5. Stress test equipment qualification and routine verification 13
16 5.1. Overview of required HBM tester evaluations 13
17 5.2. Measurement procedures 14
18 5.2.1. Reference pin pair determination 14
19 5.2.2. Waveform capture with current probe 14
20 5.2.3. Determination of waveform parameters 15
21 5.2.4. High voltage discharge path test 18
22 5.3. HBM tester qualification 18
23 5.3.1. HBM ESD tester qualification requirements 18
24 5.3.2. HBM tester qualification procedure 18
25 5.4. Test fixture board qualification for socketed testers 19
26 5.5. Routine waveform check requirements 20
27 5.5.1. Standard routine waveform check description 20
28 5.5.2. Waveform check frequency 20
29 5.5.3. Alternate routine waveform capture procedure 21
30 5.6. High voltage discharge path check 21
31 5.6.1. Relay testers 21
32 5.6.2. Non-relay testers 21
33 5.7. Tester waveform records 21
34 5.7.1. Tester and test fixture board qualification records 21
35 5.7.2. Periodic waveform check records 21
36 5.8. Safety 22
37 5.8.1. Initial set-up 22
38 5.8.2. Training 22
39 5.8.3. Personnel safety 22
40 6. Classification procedure 22
41 6.1. Devices for classification 22
42 6.2. Parametric and functional testing 22
43 6.3. Device stressing 22
44 6.3.1. Device stressing methods 22
45 6.3.2. No connect pins 23
46 6.4. Pin combination stressing 23
47 6.4.1. Pin combination stressing options 23

iTeh Standards
(https://standards.iteh.ai)
Document Preview
oSIST prEN IEC 60749-26:2025
https://standards.iteh.ai/catalog/standards/sist/787de785-9b87-4f1a-b2dd-d3b6114 7e4ad/osist-pren-iec-60749-26-2025

oSIST prEN IEC 60749-26:2025

48 6.4.2. 'No-Connect' Pins 24
49 6.4.3. Supply pins 24
50 6.4.4. Non-supply pins 25
51 6.5. Pin groupings 25
52 6.5.1. Supply pin groups 25
53 6.6. Pin stress combinations 26
54 6.6.1. Pin stress combination categorization 26
55 6.6.2. Non-supply and supply to supply combinations (1, 2, … N) 28
56 6.6.3. Non-supply to non-supply combinations 29
57 6.7. Pin-pair stressing 29
58 6.8. Low-Parasitic HBM Simulator Allowance 29
59 6.9. Testing after stressing 30
60 7. Failure criteria 30
61 8. Component classification 30
62 Annex A (informative) Cloned non-supply (I/O) pin sampling test method 31
63 A.1 Purpose and overview 31
64 A.2 Pin sampling overview and statistical details 31
65 A.3 IC product selections 32
66 A.4 Randomly selecting and testing cloned I/O pins 33
67 A.5 Determining if sampling can be used with the supplied Excel spreadsheet 33
68 A.5.1 Using the supplied Excel spreadsheet 33
69 A.5.2 Without using the Excel spreadsheet 33
70 A.6 HBM testing with a sample of cloned I/O pins 34
71 A.7 Examples of testing with sampled cloned I/Os 34
72 Annex B (informative) Determination of withstand thresholds for pin or pin-combination
73 subsets 37
74 B.1 Introduction 37
75 B.2 Testing procedures 37
76 B.3 Restrictions 38
77 B.4 Example of using subset withstand threshold data 38
78 Annex C (informative) HBM test equipment parasitic properties 39
79 C.1 Optional trailing pulse detection equipment / apparatus 39
80 C.2 Optional pre-pulse voltage rise detection test equipment 40
81 C.3 Optional Pre-HBM Current Spike Detection Equipment 42
82 C.4 Open-relay tester capacitance parasitics 43
83 C.5 Test to determine if an HBM simulator is a low-parasitic simulator 44
84 Annex D (informative) HBM test method flow chart 46
85 Annex E (informative) Failure window detection testing methods 49
86 E.1 Methodology 49
87 E.2 Combined Withstand Threshold Method and Window Search 49
88 E.3 Failure Window Detection with a Known Withstand Threshold 49
89 Bibliography 51
90

91 Figure 1 – Simplified HBM simulator circuit with loads 13
92 Figure 2 – Current waveform through shorting wires 16

iTeh Standards (https://standards.iteh.ai) Document Preview
oSIST prEN IEC 60749-26:2025
https://standards.iteh.ai/catalog/standards/sist/787de785-9b87-4f1a-b2dd-d3b61f47e4ad/osist-pren-iec-60749-26-2025

oSIST prEN IEC 60749-26:2025

93 Figure 3 – Current waveform through a 500 Ω resistor 17
94 Figure 4 – Peak current short circuit ringing waveform 18
95 Figure A.1 – SPL, V1, VM, and z with the Bell shape distribution pin failure curve 32
96 Figure A.2 – I/O sampling test method flow chart 36
97 Figure C.1 – Diagram of trailing pulse measurement setup 39
98 Figure C.2 – Positive stress at 4 000 V 40
99 Figure C.3 – Negative stress at 4 000 V 40
100 Figure C.4 – Illustration of measuring voltage before HBM pulse with a Zener diode or
101 a device 41
102 Figure C.5 – Example of voltage rise before the HBM current pulse across a 9,4 V
103 Zener diode 41
104 Figure C.6 – Optional Pre-Current Pulse Detection Equipment/Apparatus 42
105 Figure C.7 – Positive Stress at 1000 V 43
106 Figure C.8 – Diagram of a 10-pin shorting test device showing current probe 45
107 Figure D.1 – HBM test method flow chart *(1 of 3,* HBM Classification Procedure*)* 46
108
109 Table 1 – Waveform specification 20
110 Table 2 – Preferred pin combinations sets 27
111 Table 3 – Alternative pin combinations sets 27
112 Table 4 – HBM ESD component classification levels 30
113 Table.B.1. Inclusion of Lower ESD Level High-Speed Pin Data ESD Information for
114 Handling of ESDS in an ESD Protected Area (Required) 38
115
116

iTeh Standards
(https://standards.iteh.ai)
Document Preview
oSIST prEN IEC 60749-26:2025
https://standards.iteh.ai/catalog/standards/sist/787de785-9b87-4f1a-b2dd-d3b61f47e4ad/osist-pren-iec-60749-26-2025

oSIST prEN IEC 60749-26:2025

INTERNATIONAL ELECTROTECHNICAL COMMISSION

____

SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS –

Part 26: Electrostatic discharge (ESD) sensitivity testing – Human body model (HBM)

FOREWORD

1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
2) The formal decisions or agreements of IEC on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested IEC National Committees.
3) IEC Publications have the form of recommendations for international use and are accepted by IEC National Committees in that sense. While all reasonable efforts are made to ensure that the technical content of IEC Publications is accurate, IEC cannot be held responsible for the way in which they are used or for any misinterpretation by any end user.
4) In order to promote international uniformity, IEC National Committees undertake to apply IEC Publications transparently to the maximum extent possible in their national and regional publications. Any divergence between any IEC Publication and the corresponding national or regional publication shall be clearly indicated in the latter.
5) IEC itself does not provide any attestation of conformity. Independent certification bodies provide conformity assessment services and, in some areas, access to IEC marks of conformity. IEC is not responsible for any services carried out by independent certification bodies.
6) All users should ensure that they have the latest edition of this publication.
7) No liability shall attach to IEC or its directors, employees, servants or agents including individual experts and members of its technical committees and IEC National Committees for any personal injury, property damage or other damage of any nature whatsoever, whether direct or indirect, or for costs (including legal fees) and expenses arising out of the publication, use of, or reliance upon, this IEC Publication or any other IEC Publications.
8) Attention is drawn to the Normative references cited in this publication. Use of the referenced publications is indispensable for the correct application of this publication.
9) Attention is drawn to the possibility that some of the elements of this IEC Publication may be the subject of patent rights. IEC shall not be held responsible for identifying any or all such patent rights.

iTeh Standards
(https://standards.iteh.ai)
Document Preview
oSIST prEN IEC 60749-26:2025

International Standard IEC 60749-26 has been prepared by IEC technical committee 47: Semiconductor devices in collaboration with technical committee 101: Electrostatics.

This fifth edition cancels and replaces the fourth edition published in 2018. This edition constitutes a technical revision. This standard is based upon ANSI/ESDA/JEDEC JS-001-2023. It is used with permission of the copyright holders, ESD Association and JEDEC Solid state Technology Association.

This edition includes the following significant technical changes with respect to the previous edition:

a) new definitions have been added
b) text has been added to clarify the designation of and allowances resulting from "low parasitics". The new designation includes the maximum number of pins of a device that can pass the test procedure.

oSIST prEN IEC 60749-26:2025

171 The text of this International Standard is based on the following documents:

FDIS	Report on voting
47/xxxx/FDIS	47/yyyy/RVD

172

173 Full information on the voting for the approval of this International Standard can be found in the
174 report on voting indicated in the above table.

175 The language used for the development of this International Standard is English.

176 This document has been drafted in accordance with the ISO/IEC Directives, Part 2, and
177 developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC
178 Supplement, available at www.iec.ch/members_experts/refdocs. The main document types
179 developed by IEC are described in greater detail at www.iec.ch/publications.

180

181 A list of all parts in the IEC 60749 series, published under the general title *Semiconductor*
182 *devices – Mechanical and climatic test methods*, can be found on the IEC website.

183 The committee has decided that the contents of this document will remain unchanged until the
184 stability date indicated on the IEC website under "http://webstore.iec.ch" in the data related to
185 the specific document. At this date, the document will be

186 • reconfirmed,
187 • withdrawn,
188 • replaced by a revised edition, or
189 • amended.

iTeh Standards
(https://standards.iteh.ai)
Document Preview
oSIST prEN IEC 60749-26:2025
https://standards.iteh.ai/catalog/standards/sist/787de785-9b87-4f1a-b2dd-d3b61f47e4ad/osist-pren-iec-60749-26-2025

190

IMPORTANT – The 'colour inside' logo on the cover page of this publication indicates that it contains colours which are considered to be useful for the correct understanding of its contents. Users should therefore print this document using a colour printer.

191

192

oSIST prEN IEC 60749-26:2025

193 **SEMICONDUCTOR DEVICES –**
194 **MECHANICAL AND CLIMATIC TEST METHODS –**
195
196 **Part 26: Electrostatic discharge (ESD) sensitivity testing –**
197 **Human body model (HBM)**
198
199
200

201 ## 1. Scope

202 This part of IEC 60749 establishes the procedure for testing, evaluating, and classifying
203 components and microcircuits according to their susceptibility (sensitivity) to damage or
204 degradation by exposure to a defined human body model (HBM) electrostatic discharge (ESD).

205 The purpose of this document is to establish a test method that will replicate HBM failures and
206 provide reliable, repeatable HBM ESD test results from tester to tester, regardless of component
207 type. Repeatable data will allow accurate classifications and comparisons of HBM ESD
208 sensitivity levels.

209 ESD testing of semiconductor devices is selected from this test method, the machine model
210 (MM) test method (see IEC 60749-27) or other ESD test methods in the IEC 60749 series.
211 Unless otherwise specified, this test method is the one selected.

iTeh Standards
(https://standards.iteh.ai)
Document Preview

212 ## 2. Normative references

213 The following documents are referred to in the text in such a way that some or all of their content
214 constitutes requirements of this document. For dated references, only the edition cited applies.
215 For undated references, the latest edition of the referenced document (including any
216 amendments) applies.

oSIST prEN IEC 60749-26:2025
https://standards.iteh.ai/catalog/standards/sist/787de785-9b87-4f1a-b2dd-d3b61f47e4ad/osist-pren-iec-60749-26-2025

217 IEC 60749-28, *Semiconductor devices – Mechanical and climatic test methods – Part 28:*
218 *Electrostatic discharge (ESD) sensitivity testing – Machine model (MM)*

219 ## 3. Terms and definitions

220 For the purposes of this document, the following terms and definitions apply.

221 ISO and IEC maintain terminological databases for use in standardization at the following
222 addresses:

223 • IEC Electropedia: available at http://www.electropedia.org/
224 • ISO Online browsing platform: available at http://www.iso.org/obp

225 **3.1.**
226 **above-passivation layer**
227 **APL**
228
229 A low-impedance metal plane built on the surface of a die, above the passivation layer, which
230 connects a group of bumps or pins (typically power or ground).

231 Note 1 to entry This structure is sometimes referred to as a redistribution layer (RDL). There may be multiple APLs
232 (sometimes referred to as Islands) for a power or ground group.
233
234
235

oSIST prEN IEC 60749-26:2025

236 **3.2.**
237 **associated non-supply pin**
238 non-supply pin (typically an I/O pin) associated with a supply pin group

239 Note 1 to entry A non-supply pin is considered to be associated with a supply pin group if either:

240 a) the current from the supply pin group (i.e., VDDIO) is required for the function of the electrical circuit(s)
241 (I/O driver) that connect(s) (high/low impedance) to that non-supply pin;

242 b) a parasitic path exists between non-supply and supply pin group (e.g., open-drain type non-supply pin to a VCC
243 supply pin group that connects to a nearby N-well guard ring).

244 **3.3.**
245 **cloned non-supply (I/O) pin**
246 set of input, output or bidirectional pins using the same I/O cell and electrical schematic and
247 sharing the same associated supply pin group(s) including ESD power clamp(s)

248 **3.4.**
249 **component**
250 item such as a resistor, diode, transistor, integrated circuit or hybrid circuit

251 **3.5.**
252 **component failure**
253 condition in which a tested component does not meet one or more specified static or dynamic
254 data sheet parameters

255 **3.6.**
256 **coupled non-supply pin pair**
257 two pins that have an intended direct current path (such as a pass gate or resistors, such as
258 differential amplifier inputs, or low voltage differential signalling (LVDS) pins), including
259 analogue and digital differential pairs and other special function pairs (e.g., D+/D-,
260 XTALin/XTALout, RFin/RFout, TxP/TxN, RxP/RxN, CCP_DP/CCN_DN, etc.)

iTeh Standards (https://standards.iteh.ai) Document Preview oSIST prEN IEC 60749-26:2025

261 **3.7.**
262 **data sheet parameters**
263 static and dynamic component performance data supplied by the component manufacturer or
264 supplier

265 **3.8.**
266 **exposed pad**
267 exposed metal plate on an IC package, connected to the silicon substrate and acting as a heat
268 sink. This metal plate may or may not be electrically connected to the die. The exposed pad
269 may be categorized as either supply, non-supply or no-connect

270 **3.9.**

271 **3.10.**
272 **feedthrough**
273 direct or indirect (via a series resistor) connection from a pad cell layout. This connection may
274 allow additional elements, not included in the pad cell, to make electrical connections to the
275 bond pad (see Annex A). This is not to be confused with the term feed-through used in Clause
276 5 which refers to test boards.

277 **3.11.**
278 **failure window**
279 intermediate range of stress voltages that can induce failure in a particular device type, when
280 the device type can pass some stress voltages both higher and lower than this range

281 Note 1 to entry: A component with a failure window can pass a 500 V test, fail a 1 000 V test and pass a 2 000 V
282 test. The withstand voltage of such a device is 500 V.

oSIST prEN IEC 60749-26:2025

283 **3.12.**
284 **human body model electrostatic discharge**
285 **HBM ESD**
286 ESD event meeting the waveform criteria specified in this document, approximating the
287 discharge from the fingertip of a typical human being to a grounded device

288 **3.13.**
289 **HBM ESD tester**
290 HBM simulator
291 equipment that applies an HBM ESD to a component

292 **3.14.**
293 I_{ps}
294 peak current value determined by the current at time t_{max} on the linear extrapolation of the
295 exponential current decay curve, based on the current waveform data over a 40 nanosecond
296 period beginning at t_{max}

297 SEE: Figure 2 a).

298 **3.15.**
299 I_{psmax}
300 highest current value measured including the overshoot or ringing components due to internal
301 test simulator RLC parasitics

302 SEE: Figure 2 a).

iTeh Standards
(https://standards.iteh.ai)
Document Preview

303 **3.16.**
304 **no connect pin**
305 package interconnection that is not electrically connected to a die

306 EXAMPLE: Pin, bump, ball interconnection.

oSIST prEN IEC 60749-26:2025
https://standards.iteh.ai/catalog/standards/sist/787de785-9b87-4f1a-b2dd-d3b61f47e4ad/osist-pren-iec-60749-26-2025

307 Note 1 to entry: There are some pins which are labelled as no connect, which are actually connected to the die and
308 should not be classified as a no connect pin.

309 **3.17.**
310 **non-socketed tester**
311 HBM simulator that makes contact to the device under test (DUT) pins (or balls, lands, bumps
312 or die pads) with test probes rather than placing the DUT in a socket

313 **3.18.**
314 **non-supply pin**
315 pin that is not categorized as a supply pin or no connect

316 Note 1 to entry This includes pins such as input, output, offset adjusts, compensation, clocks, controls, address,
317 data, Vref pins and VPP pins on EPROM memory. Most non-supply pins transmit or receive information such as
318 digital or analogue signals, timing, clock signals, and voltage or current reference levels.

319 **3.19.**
320 **package plane**
321 low impedance metal layer built into an IC package connecting a group of bumps or pins
322 (typically power or ground)

323 Note 1 to entry: There may be multiple package planes (sometimes referred to as islands) for each power and
324 ground group.

325 **3.20.**
326 **pre-pulse voltage**
327 voltage occurring at the device under test (DUT) just prior to the generation of the HBM current
328 pulse

oSIST prEN IEC 60749-26:2025

329 SEE: Clause C.2.

330 **3.21.**
331 **pulse generation circuit**
332 dual polarity pulse source circuit network that produces a human body discharge current
333 waveform

334 Note 1 to entry The circuit network includes a pulse generator with its test equipment internal path up to the contact
335 pad of the test fixture. This circuit is also referred to as dual polarity pulse source.

336 **3.22.**
337 **ringing**
338 high frequency oscillation superimposed on a waveform

339 **3.23.**
340 **shorted non-supply pin**
341 any non-supply pin (typically an I/O pin) that is metallically connected (typically $< 3\ \Omega$) on the
342 chip or within the package to another non-supply pin (or set of non-supply pins)

343 **3.24.**
344 **socketed tester**
345 HBM simulator that makes contact to DUT pins (or balls, lands, bumps or die pads) using a
346 DUT socket mounted on a test fixture board

347 **3.25.**
348 **specification limit**
349 **SPL**
350 HBM specification limit, or target specification level and is the value set by customer
351 requirement or internal target (See Annex A)

iTeh Standards (https://standards.iteh.ai) Document Preview

352 **3.26.**
353 **spurious current pulse**
354 small HBM shaped pulse that follows the main current pulse, and is typically defined as a
355 percentage of I_{psmax}

oSIST prEN IEC 60749-26:2025
https://standards.iteh.ai/catalog/standards/sist/787de785-9b87-4f1a-b2dd-d3b61f47e4ad/osist-pren-iec-60749-26-2025

356 **3.27.**
357 **step-stress hardening**
358 ability of a component subjected to increasing ESD voltage stresses to withstand higher stress
359 levels than a similar component not previously stressed

360 EXAMPLE: A component can fail at 1 000 V if subjected to a single stress, but fail at 3 000 V if stressed
361 incrementally from 250 V.

362 **3.28.**
363 **supply pin**
364 any pin that provides current to a circuit

365 Note 1 to entry: Supply pins typically transmit no information (such as digital or analogue signals, timing, clock
366 signals, and voltage or current reference levels). For the purpose of ESD testing, power and ground pins are treated
367 as supply pins.

368 **3.29.**
369 **test fixture board**
370 specialized circuit board, with one or more component sockets, which connects the DUT(s) to
371 the HBM simulator

372 **3.30.**
373 t_{max}
374 time when I_{ps} is at its maximum value (I_{psmax})

oSIST prEN IEC 60749-26:2025

375 SEE: Figure 2 a).

376 **3.31.**
377 **trailing current pulse**
378 current pulse that occurs after the HBM current pulse has decayed

379 Note 1 to entry: A trailing current pulse is a relatively constant current often lasting for hundreds of microseconds.

380 SEE: Clause C.1.

381 **3.32.**
382 **two-pin HBM tester**
383 low parasitic HBM simulator that tests DUTs in pin pairs where floating pins are not connected
384 to the simulator thereby eliminating DUT-tester interactions from parasitic tester loading of
385 floating pins

386 **3.33.**
387 **V1**
388 maximum HBM stress voltage step where all of the selected cloned non-supply pins pass (see
389 Annex A)

390 **3.34.**
391 **V2**
392 minimum HBM stress voltage step where all the selected cloned non-supply pins fail (see Annex
393 A)

iTeh Standards
(https://standards.iteh.ai)
Document Preview

394 **3.35.**
395 **VM**
396 minimum HBM stress voltage step where 50% or greater of the selected cloned non-supply pins
397 fail (see Annex A)

oSIST prEN IEC 60749-26:2025
https://standards.iteh.ai/catalog/standards/sist/787de785-9b87-4f1a-b2dd-d3b61f47e4ad/osist-pren-iec-60749-26-2025

398 **3.36.**
399 **withstand voltage**
400 highest voltage level that does not cause device failure

401 Note 1 to entry: The device passes all tested lower voltages (see failure window).

402

403 4. Apparatus and required equipment

404 4.1. Waveform verification equipment

405 All equipment used to evaluate the tester shall be calibrated in accordance with the
406 manufacturer's recommendation. This includes the oscilloscope, current transducer and high
407 voltage resistor load. Maximum time between calibrations shall be one year. Calibration shall
408 be traceable to national or international standards.

409 Equipment capable of verifying the pulse waveforms defined in this standard test method
410 includes, but is not limited to, an oscilloscope, evaluation loads and a current transducer.

411 4.2. Oscilloscope

412 A digital oscilloscope is recommended but analogue oscilloscopes are also permitted. In order
413 to ensure accurate current waveform capture, the oscilloscope shall meet the following
414 requirements:

415 a) minimum sensitivity of 100 mA per major division when used in conjunction with the current
416 transducer specified in 4.4;

oSIST prEN IEC 60749-26:2025

417 b) minimum bandwidth of 350 MHz;
418 c) for analogue scopes, minimum writing rate of one major division per nanosecond.

419 **4.3. Additional requirements for digital oscilloscopes**

420 Where a digital oscilloscope is used, the following additional requirements apply:

421 a) recommended channels: 2 or more;
422 b) minimum sampling rate: 10^9 samples per second;
423 c) minimum vertical resolution: 8-bit;
424 d) minimum vertical accuracy: ± 2,5 %;
425 e) minimum time base accuracy: 0,01 %;
426 f) minimum record length: 10^3 points.

427 **4.4. Current probe**

428 a) minimum bandwidth of 200 MHz;
429 b) peak pulse capability of 12 A;
430 c) rise time of less than 1 ns;
431 d) capable of accepting a solid conductor as specified in 4.5;
432 e) provides an output voltage per signal current as required in 4.2
433 (this is usually between 1 mV/mA and 5 mV/mA.);
434 f) low-frequency 3 dB point below 10 kHz (e.g., Tektronix CT-2[1]) for measurement of decay
435 constant t_d (see 5.2.3.2, Table 1, and note below).

436 NOTE Results using a current probe with a low-frequency 3 dB point of 25 kHz (e.g., Tektronix CT-1[1]) to
437 measure decay constant t_d are acceptable if t_d is found to be between 130 ns and 165 ns.

438 **4.5. Evaluation loads**

iTeh Standards (https://standards.iteh.ai) Document Preview oSIST prEN IEC 60749-26:2025 https://standards.iteh.ai/catalog/standards/sist/...747e4ad/osist-pren-iec-60749-26-2025

439 Two evaluation loads are necessary to verify the tester functionality:

440 a) Load 1: A solid 18 AWG to 24 AWG (non-US standard wire size 0,25 mm^2 to 0,75 mm^2
441 cross-section) tinned copper shorting wire as short as practicable to span the distance
442 between the two farthest pins in the socket while passing through the current probe or long
443 enough to pass through the current probe and contacted by the probes of the non-socketed
444 tester.
445 b) Load 2: A (500 ± 5) Ω, minimum 4 000 V voltage rating.

446 **4.6. Attenuator**

447 A 20.0 dB attenuator with a precision of ± 0.5 dB, at least 1 GHz bandwidth, and an impedance
448 of 50 Ω ± 5 Ω.

449 **4.7. Human body model simulator**

450 A simplified schematic of the HBM simulator or tester is given in Figure 1. The performance of
451 the tester is influenced by parasitic capacitance and inductance. Thus, construction of a tester
452 using this schematic does not guarantee that it will provide the HBM pulse required for this

[1] Tektronix CT-1 and CT-2 are the trade names of products supplied by Tektronix, Inc.

This information is given for the convenience of users of this document and does not constitute an endorsement by IEC of the products named. Equivalent products may be used if they can be shown to lead to the same results.