SLOVENSKI STANDARD

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Metode in osnutki standardov za dinamično določanje lastnosti in preskušanje analogno-digitalnih pretvornikov (DYNAD)

Methods and draft standards for the dynamic characterization and testing of analogue to digital converters (DYNAD)

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Methods and draft standards for the dynamic characterization and testing of analog to digital converters (DYNAD)

This European Specification was approved by CENELEC on 1998-10-16.

CENELEC members are required to announce the existence of this ES in the same way as for an EN and to make the ES available promptly at national level in an appropriate form. It is permissible to keep conflicting national standards in force.

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CENELEC

European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

Central Secretariat: rue de Stassart 35, B - 1050 Brussels

Ref. No. ES 59006:1998 E

Foreword

This European Specification was prepared by a consortium*.

It was submitted to the CENELEC combined questionnaire and vote procedure and was approved as ES 59006 on 1998-10-16.

The following date was fixed:

- latest date by which the existence of the ES has to be announced at national level (doa) 1999-04-01

1. OBJECTIVES

The relevance of digital signal processing techniques in professional and consumer systems is steadily growing, and this makes analog -to -digital converters (ADC) key components in today's electronics. Both as independent chips and as cells of complex mixed signal circuits, they represent a market in rapid development, and manufacturers are offering devices which are more and more efficient in terms of speed, resolution, power consumption.

While a considerable effort has been produced towards the definition of blank detail specifications, the standardization of ADC test procedures is not so well developed. In particular, (see list of standards below) IEC draft 47A(Secretariat)231 covers only quasi- static operation, while it is well known that dynamic ADC operation is the main concern of end users, since the converters' performances strongly depend on the signal frequency. IEEE Std 1057 provides guidelines on this subject, but does not define the measurement setup and the data processing steps with the detail required to obtain consistent results at the level required by state of the art converters.

In this project, two leading industries active in the fields of systems and components team with three universities and research labs for carrying out research on innovative aspects of this measurement domain.

A first aim of this project is contributing to the improvement of the European rules concerning analog- to-digital converters and sample- and- hold circuits. This is of course in view of a recognition from CENELEC, and fits the present contingency, where a draft concerning static measurement methods for ADC's (document 47A(Secretariat)231 is being considered for inclusion in the IEC/CEI norms. The project aims at integrating and complementing that document for the part concerning dynamic testing, by proposing a list of parameters specifying in general the dynamic behaviour of the converter and indicating in detail the measurement conditions and the data processing algorithms.

A second aim is to investigate and propose new test methods to circumvent the limits of the measurement instrumentation, which is strongly challenged by today's high resolution, high speed converters, to measure particular parameters required for specific applications and to diagnose problems in new converter designs, on the basis of the a priori knowledge of their inner architecture.

A final objective is to provide the users of ADCs and S&Hs with information on how to use such components reliably, by suggesting appropriate choices concerning board design and the selection of components and materials. This will ultimately help improving production yield and product quality, particularly for medium-small industries which may more confidently make use of state of the art conversion products.

Emphasis is placed on is the divulgation of the knowledge concerning the specification of ADC and sample and hold circuits and their testing at bench or with general purpose testers, with the primary objective of reducing system design costs.

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* The consortium consists of:

- Università di Parma, Dipartimento di ingegneria dell'informazione "UNIPR", IT.
- Thomson-CSF technologies et methodes, Analog and microwave dep. "TTM", FR.
- Italtel S.p.A, Quality dep. "ITALTEL", IT.
- SIEMENS, Entwicklungszentrum für Mikroelectronik G.m.b.H. "SIEMENS EZM", AT.
- Ecole nationale supérieure d'électronique et de radioélectricité, Université Bordeaux, Laboratoire de l'étude de l'intégration des circuits et systèmes "ENSERB", FR.
- Instituto de engenheria de sistemas e de computadores, Dep. CAD e microelectronica "INESC", PT.

STANDARDS CONCERNING ADCs

IEC/CEI
Semiconductor devices- Integrated circuits- Part 4 Interface integrated circuits
Section 1- Blank Detail Specification for linear digital to analog converters (1993)
IEC 748-4-1/QC 790303.
Section 2- Blank Detail Specification for linear analog to digital converters (1993)
IEC 748-4-2/QC 790304.

Draft 47A(Secretariat)231: Measuring methods of linear ADC and DAC (1990).

CENELEC
Specification generique: Circuits integres monolithiques
(1990) CECC 90000 (NF C 86-020)
(1992) CECC 90000-1 Modification
Specification intermediaire: Circuits integres monolithiques d' interface
(1987) CECC 90300 (NF C 86-900)

MIL
MIL-M-38510/132

JEDEC
JEDEC Standard n.99 Addendum N.1
Terms, definitions and letter symbols for analog-to- digital and digital-to- analog converters

IEEE
IEEE Std 1057 (1989)
Draft American National Standard
Trial-use standard for digitizing waveform recorders.

IEEE Std 746-1984
IEEE Standard for Performance Measurements of A/D and D/A converters for PCM Television Video Circuits

2. WORK CONTENT

The work initially proposes (WP1) to stock the dynamic test methods best documented in the literature, hereafter referred to as "classical", answering in detail a number of open questions concerning their implementation and comparing their efficiency, and to prepare a draft norm on dynamic characterization of ADCs. Measurement techniques for the evaluation of sampling jitter, a critical topic not adequately covered by the literature, will also be developed.
For one of the methods, the feasibility of an hardware preprocessing to reduce test costs will be investigated, and a dedicated hardware will be implemented in case of positive outcome.

A dedicated workpackage (WP2) will produce a handbook with guidelines for the design of boards containing high performance converters, and in particular test boards, compacting in a single reference document a variety of information which it would be difficult to gather for individuals or small industries. This will provide to end users a guide on how to use ADCs and S/Hs correctly, finally increasing system reliability, both by decreasing the risk of component damage and by improving the information content of the converted data.
The package will also cover the design and implementation of filters for improving the spectral purity of the signal sources used for ADC test, and the specific implementation problems encountered when the converter is tested on automatic test equipment (ATE).

Novel test methods and the measurement of parameters required by specific applications (e.g. digital audio or data transmission) are covered by workpackage WP3, while sample and hold characterization is the object of WP4.

It is worth stressing that the measurement techniques to be developped will allow accurate determination of parameters like aperture time uncertainty for sample and hold circuits, or intrinsic sampling jitter for ADCs. These, besides indicating converter performance, may convey, as noise parameters, sensible reliability information. Other proposed measurements, like bit-error rate, time-frequency analysis of the converter response (drift analysis) or temperature behaviour may bring indications on both component reliability and immunity from environmental conditions. In this respect, many of the developments of this project may be regarded as necessary tools for component and system reliability studies.

The last two workpackages concern the draft normative presentation (WP5) and the dissemination of the knowledge gathered during the project (WP6).

The six workpackages:

WP 1 CLASSICAL TEST DATA ANALYSIS
WP 2 TEST HARDWARE
WP 3 SPECIAL PURPOSE TEST PROCEDURES AND PERFORMANCE PARAMETERS
WP 4 TEST PROCEDURES FOR SAMPLE AND HOLD CIRCUITS
WP 5 DRAFT NORMATIVES
WP 6 DISSEMINATION

are discussed in detail in the following sections.

2.1 Workpackage 1 (WP leader: Coordinator) CLASSICAL TEST DATA ANALYSIS

Three dynamic test methods are generally accepted: they consist of applying a spectrally pure sinewave to the ADC input and analyzing the output code words in the time domain, or in the frequency domain or by statistical techniques. This package deals with the processing of the data collected during the test. While excellent material is available in the literature, the information is somewhat scattered, and it is necessary to bring together the available knowledge, rigorously comparing the various procedures reported one against the other. Just to mention some of the problems to be fixed, estimation of the input sinewave parameters, choice of the optimization algorithm required for time- domain analysis, coherence of the results provided by different test methods at the highest signal frequencies. Despite the number of papers in this field, a sensible amount of work is still required to achieve the knowledge level allowing a detailed specification of the data processing procedures.

The activity will focus on the determination of performance parameters of interest for general purpose converters (such as integral and differential non- linearity (INL, DNL), effective number of bits (ENB), total harmonic distortion (THD), sampling jitter). The sampling jitter measurement will be investigated with the care required

by a critical parameter, difficult to be measured.
For each of the measurement techniques described below, the instrumentation set-up will be defined, taking into account ADC speed and resolution. For one of them, a dedicated hardware instrument will probably be implemented.
For the various analyses, typical test applications will be presented on three or four types of industrial A/D converters, like successive approximation, flash, subranging or sigma delta converters.

Action 1.1 Time domain data analysis
Partners 2,4

This analysis is based on the study of the ADC output codes obtained at regularly spaced, known sampling instants. The best fitting curve (sinusoid) is then determined by least squares error minimization techniques. By computing the r.m.s. difference between the best fitting curve and the data, it is possible to deduce the Signal to Noise plus Distortion Ratio (SNDR), and the corresponding Effective Number of Bits (ENB).
The action has to define:
- the best fitting algorithm (optimizing both precision and computation speed);
- the procedure for estimating SNDR and ENB;
- the algorithm for rearranging the collected data as a function of the input sinewave phase in one single period of the signal, in order to point out possible problems during the acquisition and spurious codes generated by the A/D converter;
- the instrumentation set-up (in particular, the clock and signal frequencies must be known with extreme precision).

Finally, the measurements obtained with an input sinewave spanning the input range of the converter will be correlated with measurements obtained by superimposing a relatively small sinusoid to a static bias, and varying this bias so as to span the conversion range.

The action will also compare two methods for measuring jitter and for separating the contribution of the sinewave and the clock generator from the intrinsic sampling jitter of the converter. The corresponding measurement procedures will be defined.

The action may be broken down as follows:

1.1.1 Sinewave fitting, SNDR and ENB.
.1 Choice of the minimization algorithm.
.2 Choice of the initial guess.
.3 Minimum number of samples required.
.4 Large signal vs. small signal testing.
.5 Suggested hardware setup.

1.1.2 Jitter measurements.
.1 Sampling at zero slope of a sinewave input signal.
.2 Double beat frequency method.
.3 Comparison between the two methods.

Manpower: 7 mm
Interdependencies: This action provides inputs to actions 1.4, 1.5, 1.6 and 2.2
Time scale: months 1 to 12

Action 1.2 Frequency domain data analysis
Partners 2,4

The basis of the method is the Finite Fourier Transform, by means of which a finite set of samples of the input sinewave, obtained at regular time intervals, is transformed into a finite set of spectral components in the frequency domain. Several parameters used for the characterization of A/D converters may be extracted from the resulting spectrum: namely, Total Harmonic Distortion (THD), Signal to Noise plus Distortion Ratio (SNDR) and Signal to Noise Ratio (SNR).
The two main issues hampering the use of this methods are aliasing and spectral leakage. Because of aliasing, harmonic components of the signal do not appear in the natural order, which has to be reconstructed. Spectral

leakage, related to the artificial introduction of discontinuities when the observation window does not contain an integer number of signal periods, can be cured either by synchronization or by use of suitable weighting windows.

The action has to define:

- the reordering algorithm, the optimal window to be used and the error introduced by the window on SNR estimation, in the case of asynchronous sampling;
- the precise equations to be used for evaluating the spectral characterization parameters, SNDR, THD, SNR;
- the minimum number of samples, depending on the converter's resolution;
- the correction to be applied to the ENB parameter depending on the amplitude of the input signal (full scale or not).
- the correlation between large signal measurements (sinewave spanning the entire input range) and small signal measurements (small sinewave superimposed to a DC offset, which may be varied so as to span the entire range).

The action will be organized as follows:

1.2.1 Synchronous sampling
1.2.2 Asynchronous sampling
.1 Windowing
1.2.3 Required number of samples, estimation of ENB
1.2.4 Large signal vs. small signal testing
1.2.5 Hardware requirements

Manpower: 8 mm
Interdependencies: This action provides inputs to actions 1.4, 1.5, 1.6 and 2.2
Time scale: months 1 to 12

Action 1.3 Statistical data analysis (histogram testing)
Coordinator, partners 2,5.

A high purity sinewave is applied to the converter's input, and a large number of samples are used to build an histogram reporting the frequency of occurrence of each code. By comparing it with the theoretical probability density function, it is possible to determine differential and integral non-linearities (DNL, INL). This requires an accurate knowledge of the input signal amplitude and offset, which may dictate the choice of a saturated input signal when the converter's architecture allows it, and the use of the cumulated histogram rather than the frequency histogram as frequently reported.

The action will define:

- the optimal algorithm for estimating amplitude and offset;
- the procedure for determining the conversion characteristic;
- the equations to be used for estimating DNL, INL and other converter parameters which may be derived from the conversion characteristic;
- the minimum number of samples to be collected depending on the sampling scheme (random, periodic or a combination of the two), the converter's resolution and the precision and confidence level required for the parameters;
- the influence of noise on the measurement.

The feasibility of reducing the processing time by an hardware preprocessor capable of eliminating the extremum data of measured code frequency histogram for a sinewave input signal will also be investigated. If the feasibility is demonstrated, an histogram board will be developped and applied for the characterization of state of the art, 8 to 14 bit A/D converters.

The action will be articulated as follows:

1.3.1 Random vs. periodic sampling, number of samples required.
.1 Saturated vs. non-saturated histogram.

1.3.2 Determination of the input sinewave parameters.
1.3.3 Determination of INL, DNL, SNDR.
1.3.4 Estimation of THD and SNR (quantization noise only).
1.3.5 Effects of additive noise and jitter.
1.3.6 Large signal vs. small signal testing.
1.3.7 Hardware requirements.
1.3.8 Hardware preprocessor feasibility and implementation.

Manpower: 20 mm
Interdependencies: This action provides inputs to actions 1.4, 1.5, 1.6 and 2.2
Time scale: months 1 to 12, except for hardware preprocessor implementation, which has to be defined according to the results of the feasibility study.

Action 1.4 Comparison of the above methods
Coordinator, partners 2,4,5

This action will demonstrate links between the parameters obtained from the three previous types of analysis. Advantages and drawbacks of each method will be pointed out, and the possible preminence of a single method, from which the complete (or an almost complete) set of characteristic parameters could be deduced, will be investigated.
A further result of the action will be a user guide indicating which parameters should be considered for a given application of the A/D converter. From this knowledge, a procedure helping the user to estimate the precision of the system including the A/D converter will be established.

The action is organized as follows:

1.4.1 Theoretical framework
1.4.2 Simulated experiments
1.4.3 Physical experiments

Manpower: 16 mm
Interdependencies: This action provides inputs to actions 1.6 and 2.2
Time scale: months 7 to 18

Action 1.5 Specification of sinewave and clock generators for the above methods
Partner 2

The quality of the input and clock signals applied during the test of an A/D converter is the most important problem for obtaining reliable results reflecting the real device performances, since these can be easily masked by poor linearity and noise in the generators. For each of the above methods, this action will define the requirements on the sinewave generator and on the clock generator as a function of the converter's resolution. Furthermore, new measurement techniques will be investigated, in particular for what concerns the clock to sinewave jitter.

The action therefore includes specification of:

1.5.1 Signal purity, stability, additive noise.
1.5.2 Jitter, phase noise, sampling clock synchronization.
1.5.3 Hardware requirements comparison

Manpower: 1 mm
Interdependencies: This action provides inputs to actions 1.6 and 2.2
Time scale: months 1 to 15

Action 1.6 Redaction of draft standards
Coordinator, partners 2,4

1.6.1 Redaction of the part of the draft norm concerning time domain analysis