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Road vehicles — Application of predictive maintenance to hardware with ISO 26262-5

Véhicules routiers — Application de la maintenance prédictive au matériel à l'aide de l'ISO 26262-5

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Contents

Page

Foreword

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This document was prepared by Technical Committee ISO/TC 22, *Road vehicles*, Subcommittee SC 32, *Electrical and electronic components and general system aspects.*

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Introduction

Hardware elements wear out or degrade with time and usage. The presence of certain faults can cause the rate of degradation to increase. If the rate of degradation exceeds critical thresholds, then a hardware element can fail during its normal expected lifespan. Addressing fault behaviours which change over time is difficult. Functional safety standards such as the ISO 26262 series have traditionally addressed degrading faults with avoidance measures and simplified assumptions of static behaviours.

Understanding of degrading faults is improving over time. Many industries are taking proactive steps to control degrading faults using predictive maintenance. Predictive maintenance can detect degrading faults and predict remaining useful life. Safety mechanisms based on predictive maintenance are not explicitly discussed in the ISO 26262 series.

This document provides a survey of current state of the art for degrading faults and predictive maintenance techniques. Approaches are presented to consider degrading faults and predictive maintenance techniques in an ISO 26262 safety argument. Much of the content is focused on semiconductors, but the concepts can be applied to other hardware elements.

Road vehicles — Application of predictive maintenance to hardware with ISO 26262-5

1 Scope

This document is intended to be applied to the usage of predictive maintenance methods for the detection of degrading faults in safety related E/E hardware elements. It applies to hardware elements developed for compliance with the ISO 26262[1] series in which degrading faults are shown to be relevant due to, for instance, the technology used.

Specific technical implementations of predictive maintenance solutions are not in scope of this document.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

ISO 26262-1, *Road vehicles — Functional safety — Part 1: Vocabulary*

3 Terms and definitions

For the purposes of this document, the terms and definitions given in ISO 26262-1 and the following apply.

ISO and IEC maintain terminology databases for use in standardization at the following addresses:

— ISO Online browsing platform: available at https://www.iso.org/obp

— IEC Electropedia: available at https://www.electropedia.org/

3.1
degrading fault
fault whose characteristics are not constant and degrade over time, that can result in an error or failure when stimulated after degradation exceeds a critical threshold

Note 1 to entry: Permanent and intermittent faults can first manifest as degrading faults. Transient faults do not manifest as degrading faults.

Note 2 to entry: Degrading faults do not create errors or failures until degradation exceeds critical thresholds. The capability to generate an error or failure is related to the current state of degradation.

Note 3 to entry: Degrading faults exhibit abnormal conditions which can cause an error or failure over time. Normal degradation does not exhibit abnormal conditions which are necessary to be classified as a fault. Normal degradation can result in a loss of functionality after expected lifespan has elapsed but cannot be considered a fault as it is not abnormal.

3.2
degrading fault detection time interval
DFDTI
timespan from the occurrence of a *degrading fault* (3.1) to its detection

3.3
degrading fault handling time interval
DFHTI
sum of the *degrading fault detection time interval* (3.2) and the *degrading fault reaction time interval* (3.4).

Note 1 to entry: The degrading fault handling time interval is a property of a *predictive maintenance* (3.5) related safety mechanism.

Note 2 to entry: The degrading fault handling time interval is considered in addition to the fault handling time interval. See Figure 4.

Note 3 to entry: The timespan from occurrence of a *degrading fault* (3.1) until it has the capability to generate an error or failure is the maximum degrading fault handling time interval that can be specified for a predictive maintenance related safety mechanism to support the functional safety concept.

Note 4 to entry: A *degrading fault* (3.1) is covered in a timely manner by the corresponding safety mechanism if there is detection and reaction within the degrading fault handling time interval.

3.4
degrading fault reaction time interval
DFRTI
timespan from the detection of a *degrading fault* (3.1) to reaching a safe state or reaching emergency operation

3.5
predictive maintenance
techniques that are used to detect *degrading faults* (3.1), predict *remaining useful life* (3.6), and react appropriately

Note 1 to entry: Approaches include the use of data driven methods such as machine learning applied locally or on a remote system. Guidance for developing safety related ML systems can be found in ISO/IEC TR 5469[2].

Note 2 to entry: Prediction of *remaining useful life* (3.6) can be used to replace a faulty element before it can cause an error or failure.

3.6
remaining useful life
RUL
length of time from the present time to the estimated time that the item or element is expected to no longer perform its intended function within desired specifications

Note 1 to entry: RUL can be estimated using *predictive maintenance* (3.5) or with other approaches.

Note 2 to entry: RUL can be estimated for expected degradation or degradation in the presence of a fault.

[SOURCE: IEEE 1856-2017[3], modified for compliance to ISO directives]

4 Abbreviated terms

ADAS	Advanced Driver Assistance System
ADS	Automated Driving System
AI	Artificial Intelligence
BEoL	Back End of Line (sometimes BEOL)
BFR	Base Failure Rate
BLM	Barrier Layer Material

CHC	Channel Hot Carrier
COTS	Commercial Off The Shelf
DC	Diagnostic Coverage
DFDTI	Degrading Fault Detection Time Interval
DFHTI	Degrading Fault Handling Time Interval
DFRTI	Degrading Fault Reaction Time Interval
DRAM	Dynamic Random Access Memory
EM	Electromigration
ESD	Electrostatic Discharge
FEoL	Front End of Line (sometimes FEOL)
FET	Field Effect Transistor
FDTI	Fault Detection Time Interval
FHTI	Fault Handling Time Interval
FTTI	Fault Tolerant Time Interval
HCI	Hot Carrier Injection
ILD	Inter-Layer Dielectric
LFM	Latent Fault Metric
ML	Machine Learning
MoL	Middle of Line (sometimes MOL)
MEoL	Middle End of Line (sometimes MEOL)
MPFDTI	Multiple Point Fault Detection Time Interval
NBTI	Negative Bias Temperature Instability
NVM	Non-Volatile Memory
PCM	Phase Change Memory
PHM	Prognostics and Health Management
RUL	Remaining Useful Life
SBD	Soft Breakdown
SHE	Self-Heating Effect
SILC	Stress-Induced Leakage Current
SM	Stress Migration
SoC	System on Chip

SPFM	Single Point Fault Metric
TDDB	Time Dependent Dielectric Breakdown
TDJD	Time Dependent Junction Degradation
TID	Total Ionizing Dose

5 Literature survey of degrading faults

5.1 General

This document reviews many technical documents to summarize the current state of the art understanding of degrading faults in industry standards and technical publications.

NOTE Terminology in the referenced publications and standards is not always aligned to terms and definitions of the ISO 26262 series. When referencing publications and standards, the terminology of the referenced work is used.

5.2 Degrading faults in industry standards

5.2.1 JEDEC JEP122H[4]

The JEDEC Solid State Technology Association is a semiconductor industry trade association and standardization body. JEDEC has over 300 companies as members and publishes electronics standards on a wide variety of topics.

JEDEC JEP122H is the latest revision on JEDEC's standard for "Failure Mechanisms and Models for Semiconductor Devices," last updated in 2016. The standard describes eighteen different failure mechanisms, classifying them as being related to the die front end of line (FEoL), die back end of line (BEoL), or packaging. Models are provided for estimating the rates of degradation per failure mode. The information provided in JEP122H is validated by a team of reliability experts from the SEMATECH/ISMI Reliability Council and supported by extensive references to technical publications.

The die FEoL failure mechanisms described by the JEP122H include:

— time dependent dielectric breakdown (TDDB) due to gate oxide breakdown;

— hot carrier Injection (HCI);

— negative bias temperature instability (NBTI);

— surface inversion due to mobile ions;

— floating gate non-volatile memory (NVM) data retention;

— localized charge trapping NVM data retention;

— phase change memory (PCM) NVM data retention.

The die BEoL failure mechanisms described by JEP122H include:

— TDDB due to ILD/low-k/mobile Cu ions;

— aluminium electromigration (EM);

— copper EM;

— aluminium and copper corrosion;

— aluminium stress migration (SM);

— copper SM.

The packaging failure mechanisms described in JEP122H include:

— fatigue failures due to temperature cycling and thermal shock;

— interfacial failures due to temperature cycling and thermal shock;

— intermetallic and oxidation failure due to high temperature;

— tin whiskers;

— ion mobility kinetics due to component cleanliness.

5.3 Degrading faults in technical publications

5.3.1 Advanced CMOS Reliability Update: Sub 20 nm FinFET Assessment[5]

Reference [5] was published by Sandia National Laboratories, a research organization of the United States Department of Energy, in 2020. The purpose of the report is to document the most critical failure modes impacting advanced semiconductor technologies using FinFET technology. FinFET based semiconductors are used for most current generation SoCs (system on chip devices), dGPUs (discrete graphics processing units), and DRAMs (dynamic random-access memories) which are used in infotainment, ADAS (advanced driver assistance systems), and ADS (automated driving system) applications. While the use of FinFET transistors enables smaller process geometries (e.g. <20 nm feature size) and faster processing, it also changes the failure mode susceptibility characteristics compared to more traditional planar transistor technologies found in 28 nm and larger process technologies.

The report provides details for the following failure modes:

— die related failure modes:
  — bias temperature instability (BTI);
  — dielectric integrity;
  — HCI;
  — BEoL, EM and stress voiding;
  — middle end of line (MEoL) concerns (also known as middle of line, or MoL);
— packaging and package-die interaction;
— integrated die design and process reliability – electrostatic discharge (ESD);
— radiation effects:
  — total ionizing dose (TID);
  — displacement damage;
  — COTS electronics and radiation effects.

The die and packaging related failure modes discussed can generally be argued to manifest as random degrading faults before becoming intermittent or permanent faults. The ESD and radiation effects can generally be argued to be systematic or transient in nature.

Also of interest is the section on reliability degradation and its impact on circuit/system performance. This section focuses on “soft” logic failures which manifest before “hard” physical failures of the semiconductor devices. As most of the degradation mechanisms discussed result in parameter degradation, it is suggested that statistical methods can be used to predict circuit failures.