



**SLOVENSKI STANDARD**  
**SIST EN 165000-5:2002**

**01-september-2002**

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**Film and hybrid integrated circuits - Part 5: Procedure for qualification approval**

Film and hybrid integrated circuits -- Part 5: Procedure for qualification approval

Integrierte Hybrid- und Schichtschaltungen -- Teil 5: Verfahren für die Bauartanerkennung

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**ICS:**

31.200

Integrirana vezja,  
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**en**

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English version

**Film and hybrid integrated circuits  
Part 5: Procedure for qualification approval**

Integrierte Hybrid- und  
Schichtschaltungen  
Teil 5: Verfahren für die  
Bauartanerkennung

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Up-to-date lists and bibliographical references concerning such national standards may be obtained on application to the Central Secretariat or to any CENELEC member.

This European Standard exists in three official versions (English, French, German). A version in any other language made by translation under the responsibility of a CENELEC member into its own language and notified to the Central Secretariat has the same status as the official versions.

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**CENELEC**

European Committee for Electrotechnical Standardization  
Comité Européen de Normalisation Electrotechnique  
Europäisches Komitee für Elektrotechnische Normung

Central Secretariat: rue de Stassart 35, B - 1050 Brussels

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### Foreword

This European Standard was prepared by the Technical Committee CENELEC/TC CECC/SC 47AX, Film and hybrid integrated circuits.

The text of the draft was submitted to the Unique Acceptance Procedure and was approved by CENELEC as EN 165000-5 on 1997-10-01.

The following dates were fixed:

- latest date by which the EN has to be implemented at national level by publication of an identical national standard or by endorsement (dop) 1998-09-01
- latest date by which the national standards conflicting with the EN have to be withdrawn (dow) 1998-09-01

This standard is intended to be read in conjunction with other parts of EN 165000 which are:

Part 1: Generic specification - Capability approval procedure

Part 2: Internal visual inspection and special tests

Part 4: Customer information, product assessment level schedules and blank detail specification

Part 4 is considered an essential document for all users; in particular it includes a helpful introductory section which is aimed at potential customers and seeks to explain the underlying philosophy upon which the whole standard is based.



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## 1. SCOPE:

This specification applies to film and hybrid integrated circuits manufactured as catalogue products or as custom built products using thick/thin film techniques and whose quality is assessed on the basis of Qualification Approval.

Test methods are selected from EN 165000-1. A Blank Detail Specification (BDS) is included to assist manufacturers and users in the preparation of detail specifications.

Related documents, preferred ratings and characteristics, and terminology are given in EN 165000-1.

## 2. RELATED DOCUMENTS

Normative references are listed in EN 165000-1, to which should be added:

CECC 00 114 part II - (RP14 part II) qualification approval of  
electronic components

## 3. QUALIFICATION APPROVAL PROCEDURES

### 3.1 General

The procedures in RP14 part II shall apply.

2.1 of EN 165000-1 applies with the exceptions given in 3.2 to 3.11.

### 3.2 Marking

1.5 of EN 165000-1 applies.

### 3.3 Validity of release for delivery

Circuits may be released under Qualification Approval subject to the following conditions:

- a) the circuits conform with the requirements of the detail specification.
- b) the circuits, their added components, piece parts and materials are traceable to original manufacturer's lot numbers.

### 3.4 Application for Qualification Approval

Application shall be made to the ONH in accordance with § 1.3 of RP14 part II. In addition, the manufacturer shall:

- a) conform with the eligibility requirements of 2.1.1 of EN 165000-1.
- b) conform with the relevant detail specification based on the Blank Detail Specification (see clause 5) and the Qualification - Product Assessment Level Schedules (Q-PALS) (see clause 4) contained in this document.

### 3.5 Structural similarity

For the purposes of assessment testing, structural similarity can be used if the testing of one representative type of circuit gives at least the same quality level for the rest of the types which are grouped together.

The CECC System Manager shall declare to the satisfaction of the ONS the method of operating the structural similarity plan within the manufacturing facilities and agree the representative type(s) from each structurally similar group.

For the Qualification Approval procedure two or more circuits can be considered structurally similar, and thus the required numbers of specimens for a test shall be selected from the combined production, when they have the same function type, use the same design rules, materials, processes and methods (for example a range of T-cell thick film attenuators using the same line of inks; or thin film D/A convertors using the same film material and same added components from the same supplier).

Only those tests not specifically excluded in the Q-PALS may be considered for structural similarity.

### 3.6 Materials, piece-parts and added components

2.1.4 of EN 165000-1 applies.

### 3.7 Initial Qualification Approval

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The schedules to be used for Qualification Approval testing on the basis of lot-by-lot and periodic testing are given in the Q-PALS tables contained in this document.

The procedure for initial Qualification Approval is given below.

The relevant Q-PALS for initial Qualification Approval, release of products (lot-by-lot tests) and maintenance of Qualification Approval (periodic tests) collectively prescribe the minimum test programme on completed circuits.

#### 1) Sampling

The sample shall be representative of the range of circuits for which approval is sought. (See 2.2.4(3) of EN 165000-1). The size of the sample and the criterion of acceptability depend on the relevant Q-PALS which it is intended to release against.

## 2) Tests

The complete series of tests specified in the relevant Q-PALS contained in this document is required for the approval of circuits covered by one detail specification. The tests shall be carried out in the order given.

Test and measurement procedures are given in clause 3 of EN 165000-1.

Samples used for group B, C & D tests shall have passed group A tests.

One failure is counted when a circuit has not satisfied the whole or a part of the tests of a group.

The approval is granted when the number of failures does not exceed the specified number of permissible failures for each group or sub-group.

### 3.8 Granting of Qualification Approval

The manufacturer shall submit a report to the ONS covering the Qualification Approval testing in accordance with the requirements of 3.7 of this document and § 1.5 of RP14 part II.

Qualification Approval shall be granted when the requirements of this document have been satisfied.

A Qualification Approval Certificate will be issued by the responsible national authority in accordance with § 1.6 of RP 14 part II.

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### 3.9 Maintenance of Qualification Approval

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#### 3.9.1 General

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Qualification Approval is maintained after successful completion of the procedures and requirements of quality conformance inspection (see 2.4.2 of EN 165000-1) with the following details:

#### 1) Design Evaluation Tests

In addition to the initial delivery lot, design evaluation tests shall be carried out at the periodicity specified in the detail specification.

#### 2) Detail Specification

The detail specification shall conform to the requirements of the BDS and Q-PALS in this document.

The manufacturer shall also have maintained continuous production, for example:

- a) there has been no change in the place of manufacture and final test;
- b) there has been no break exceeding two years in the manufacturer's declared periodic test schedule.



### 3.9.2 Changes to Qualification Approval

The manufacturer is required to notify the ONS of changes to his Qualification Approval in accordance with § 1.9 of RP14 part II and 2.3.2 a) to h) of EN 165000-1, where applicable.

*Note: All re-verification programmes are to be agreed with the ONS.*

### 3.10 Procedure in the event of a failure in a periodic test

The procedure described in § 1.8 of RP14 part II shall apply.

### 3.11 Withdrawal of Qualification Approval

The procedures in § 1.10 and § 1.11 of RP14 part II shall apply.

## 4. QUALIFICATION-PRODUCT ASSESSMENT LEVEL SCHEDULES

*Note:*

*The following eleven Q-PALS are based upon corresponding PALS in EN 165000-4.*

*Q-PALS 4, 5, 8, 9, 10 and 11 are structured to include subgroups C1 and C2 so that the schedules correspond to CECC 63000 Assessment Level K*

*The remaining Q-PALS correspond to CECC 63000 Assessment Levels L and M.*

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**Q-PRODUCT ASSESSMENT LEVEL SCHEDULE 1.****Applicability.**

This assessment schedule is intended for use with solder assembled and/or bare die, non-hermetic encapsulated, unencapsulated, cavity or non-cavity devices, which are for use in benign mechanical and temperature environments.

**Subgroup A Tests: Device Screening 100%****EN 165000-1  
Reference**

- |  |     |
|--|-----|
| 1. Electrical test @ $T_{amb}$ . Those tests in the Detail Specification which define circuit functionality. | 3.4 |
|--|-----|

**Subgroup B Tests (lot-by-lot): Device Sample Testing. IL S4 AQL 0,4%**

- |  |       |
|--|-------|
| 1. Electrical test @ $T_{amb}$ (other than those specified for Screening). | 3.4   |
| 2. External visual inspections.  | 3.3.2 |

**Subgroup C Tests (6 monthly period): Design Evaluation.**

Minimum sample 8. Accept on 0 failures.

- |   |       |
|---|-------|
| 1. Electrical test. All specified parameters @ $T_{min}$ & $T_{max}$ .* | 3.4   |
| 2. Dimensions.  | 3.3.3 |

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**Subgroup D Tests (12 monthly period): Design Evaluation.**

Minimum sample 3. Accept on 0 failures.

- |   |        |        |
|---|--------|--------|
| 1. Resistance of circuits to solder heat. | (D)    | 3.5.11 |
| 2. Solderability.                         | (ND/D) | 3.5.10 |
| 3. Robustness of terminations.            | (D)    | 3.5.12 |
| 4. Flammability.                          | (D)    | 3.5.16 |
| 5. Resistance to solvents.                | (ND)   | 3.5.15 |

\* Structural similarity rules do not apply.

**Process and Packaging requirements.**

- |  |       |
|--|-------|
| 1. Substrate fabrication = class 100 000.              |       |
| 2. Substrate assembly (bare die) = class 100 000.      |       |
| 3. E.S.D precautions (where applicable) to CECC 00015. |       |
| 4. Pre-cap visual @ IL S4 AQL 0,4% minimum.            | 3.3.1 |

**Q-PRODUCT ASSESSMENT LEVEL SCHEDULE 2.****Applicability.**

This assessment schedule is intended for use with solder assembled and/or bare die, non-hermetic encapsulated, unencapsulated, cavity or non-cavity devices, which are for use in benign mechanical and temperature environments.

**Subgroup A Tests: Device Screening 100%****EN 165000-1  
Reference**

- |  |     |
|--|-----|
| 1. Electrical test @ $T_{amb}$ . Those tests in the Detail Specification which define circuit functionality. | 3.4 |
|--|-----|

**Subgroup B Tests (lot-by-lot): Device Sample Testing. IL S4 AQL 0,4%**

- |  |       |
|--|-------|
| 1. Electrical test @ $T_{amb}$ (other than those specified for Screening). | 3.4   |
| 2. External visual inspection.   | 3.3.2 |

**Subgroup C Tests (6 monthly period): Design Evaluation.**

Minimum sample 8. Accept on 0 failures.

- |   |        |
|---|--------|
| 1. Electrical Endurance 1000 h. Release after 160 h.*                   | 3.5.14 |
| 2. Electrical test. All specified parameters @ $T_{min}$ & $T_{max}$ .* | 3.4    |
| 3. Dimensions.  | 3.3.3  |

**Subgroup D Tests (12 monthly period): Design Evaluation.**

Minimum sample 3. Accept on 0 failures.

- |   |        |        |
|---|--------|--------|
| 1. Resistance of circuits to solder heat. | (D)    | 3.5.11 |
| 2. Solderability.                         | (ND/D) | 3.5.10 |
| 3. Robustness of terminations.            | (D)    | 3.5.12 |
| 4. Flammability.                          | (D)    | 3.5.16 |
| 5. Resistance to solvents.                | (ND)   | 3.5.15 |

\* Structural similarity rules do not apply.

**Q-PRODUCT ASSESSMENT LEVEL SCHEDULE 2, continued****Process and Packaging requirements.**

1. Substrate fabrication = class 100 000.
2. Substrate assembly (bare die) = class 100 000.
3. E.S.D precautions (where applicable) to CECC 00015.
4. Pre-cap visual @ IL S4 AQL 0,4% minimum.

3.3.1

\* Structural similarity rules do not apply.

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