



International
Standard

ISO 11898-2

**Road vehicles — Controller area
network (CAN) —**

Part 2:

**High-speed physical medium
attachment (PMA) sublayer**

*Véhicules routiers — Gestionnaire de réseau de
communication (CAN) —*

*Partie 2: Sous-couche de l'unité d'accès au support à haute
vitesse (PMA)*

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Foreword

ISO (the International Organization for Standardization) is a worldwide federation of national standards bodies (ISO member bodies). The work of preparing International Standards is normally carried out through ISO technical committees. Each member body interested in a subject for which a technical committee has been established has the right to be represented on that committee. International organizations, governmental and non-governmental, in liaison with ISO, also take part in the work. ISO collaborates closely with the International Electrotechnical Commission (IEC) on all matters of electrotechnical standardization.

The procedures used to develop this document and those intended for its further maintenance are described in the ISO/IEC Directives, Part 1. In particular, the different approval criteria needed for the different types of ISO document should be noted. This document was drafted in accordance with the editorial rules of the ISO/IEC Directives, Part 2 (see www.iso.org/directives).

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This document was prepared by Technical Committee ISO/TC 22, *Road vehicles*, Subcommittee SC 31, *Data communication*.

This third edition cancels and replaces the second edition (ISO 11898-2:2016), which has been technically revised.

The main changes are as follows:

- [Clause 5](#) is restructured, the parameters are categorized by static parameter and dynamic parameter;
- Table 13 with bit rates above 1 Mbit/s and up to 2 Mbit/s is in this edition [Table 15](#) (parameter set A). Table 14 with bit rates above 2 Mbit/s and up to 5 Mbit/s is now [Table 16](#) (parameter set B). The parameter set C (see [Table 17](#) and [Table 18](#)) in this edition is newly introduced;
- [Annex A](#) in this edition is newly introduced; it specifies HS-PMAs with the SIC mode and the FAST mode. [Annex B](#) and [Annex C](#) in this edition are Annex A and Annex B in the previous edition. The content is unchanged.

A list of all parts in the ISO 11898 series can be found on the ISO website.

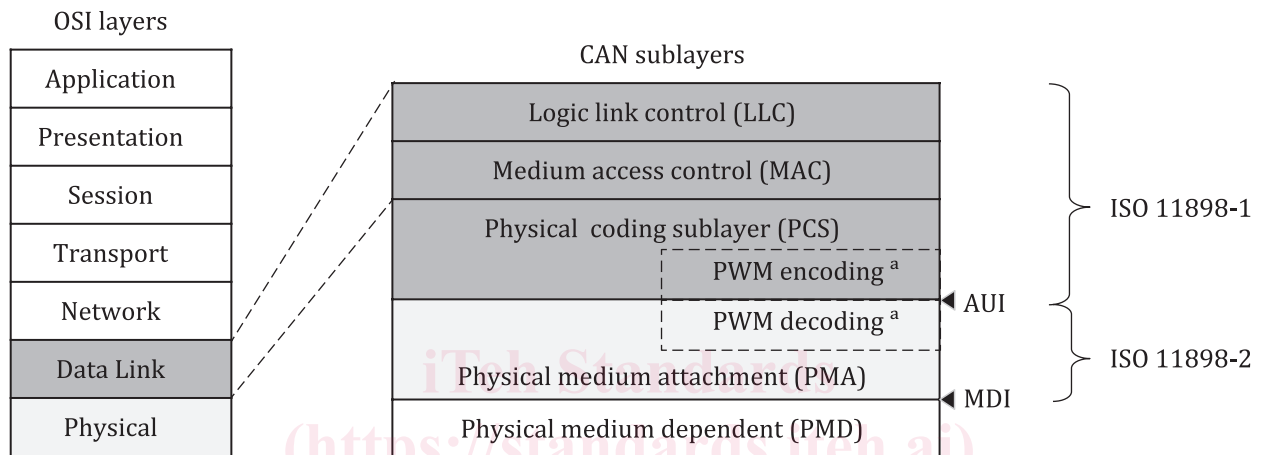
Any feedback or questions on this document should be directed to the user's national standards body. A complete listing of these bodies can be found at www.iso.org/members.html.

Introduction

The ISO 11898 series provides requirement specifications for the CAN data link layer and physical layer. It is intended for chip implementers, e.g. ISO 11898-1 for CAN protocol controllers and this document for CAN transceivers. Related conformance test plans are given in the ISO 16845 series. The CAN data link layer models the open system interconnect (OSI) data link layer; it is internally subdivided into logic link control (LLC) and medium access control (MAC). ISO 11898-1 also specifies the CAN physical coding sublayer (PCS) by means of the attachment unit interface (AUI). Optionally, the PCS also provides the PWM encoding to be linked to a CAN SIC XL transceiver, which provides the PWM decoding.

The open system interconnect (OSI) layers above the data link layer (e.g. the network layer) are not specified in the ISO 11898 series.

Figure 1 shows the relation between the OSI layers and the CAN sublayers.



Key

AUI attachment unit interface

MDI medium dependent interface

^a Only supported by CAN XL.

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Figure 1 — CAN data link and physical sublayers relation to the OSI model

Road vehicles — Controller area network (CAN) —

Part 2: High-speed physical medium attachment (PMA) sublayer

1 Scope

This document specifies physical medium attachment (PMA) sublayers for the controller area network (CAN). This includes the high-speed (HS) PMA without and with low-power mode capability, without and with selective wake-up functionality. Additionally, this document specifies PMAs supporting the signal improvement capability (SIC) mode and the FAST mode in [Annex A](#). The physical medium dependent (PMD) sublayer is not in the scope of this document.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

ISO/IEC 7498-1, *Information technology — Open Systems Interconnection — Basic Reference Model: The Basic Model*

ISO 11898-1¹⁾, *Road vehicles — Controller area network (CAN) — Part 1: Data link layer and physical signalling*

3 Terms and definitions

For the purposes of this document, the terms and definitions given in ISO/IEC 7498-1, ISO 11898-1 and the following apply.

ISO and IEC maintain terminology databases for use in standardization at the following addresses:

- ISO Online browsing platform: available at <https://www.iso.org/obp>
- IEC Electropedia: available at <https://www.electropedia.org/>

3.1 active recessive

intermediate high-speed physical medium attachment (HS-PMA) output drive with a dedicated lower than nominal impedance at transitions from dominant state or level_0 state towards the *passive recessive* (3.14) state with a dedicated duration

3.2 attachment unit interface

AUI
interface between the *physical coding sublayer (PCS)* (3.15) and the *physical medium attachment (PMA)* (3.16) sublayer

3.3 bus

shared medium of any topology

1) Third edition under preparation. Stage at the time of publication: ISO/DIS 11898-1:2024.

3.4

bus state

state of the *medium dependent interface (MDI)* (3.11), which is dominant or recessive if the *physical medium attachment (PMA)* (3.16) sublayer is in arbitration mode, or is level_0 or level_1 otherwise

Note 1 to entry: The dominant state represents the logical 0 and the recessive state represents the logical 1. During simultaneous transmission of dominant and recessive bits, the resulting bus state is dominant. When no transmission is in progress, the *bus* (3.3) is idle. During idle time, it is in recessive state.

Note 2 to entry: The level_0 state represents the logical 0, and the level_1 state represents the logical 1.

3.5

CAN_H, CAN_L

pair of ports, where $V_{CAN_H} - V_{CAN_L}$ is positive at dominant *bus state* (3.4) and level_0 bus state

3.6

edge

difference in *bus states* (3.4) between two consecutive time quanta

3.7

FAST RX mode

mode in which the *physical medium attachment (PMA)* (3.16) sublayer drives the *bus state* (3.4) recessive and the receive thresholds are adjusted to distinguish between the bus states level_0 and level_1

3.8

FAST TX mode

mode in which the *physical medium attachment (PMA)* (3.16) sublayer drives the *bus states* (3.4) level_0 and level_1, which are not able to overwrite each other

3.9

legacy implementation

HS-PMA implementation compliant with previous ISO 11898-2 editions

3.10

low-power mode

mode in which the transceiver is not capable of transmitting or receiving frames, except for the purposes of determining if a WUP or WUF is being received

3.11

MDI

medium dependent interface

electrical interface consisting of CAN_H and CAN_L, that defines the signal transfer between the *physical medium dependent (PMD)* sublayer and the *physical medium attachment (PMA)* (3.16) sublayer

3.12

nominal bit time

duration of one bit in the arbitration phase

3.13

normal-power mode

mode in which the transceiver is capable of transmitting and receiving

3.14

passive recessive

final high-speed physical medium attachment (HS-PMA) output drive with nominal impedance, also known as recessive

3.15

physical coding sublayer

PCS

sublayer of the open system interconnect (OSI) physical layer that performs bit encoding/decoding and synchronization

3.16

physical medium attachment

PMA

sublayer of the open system interconnect (OSI) physical layer that converts physical signals into logical signals and vice versa

3.17

PWM decoding

PWMD

physical medium attachment (PMA) (3.16) sublayer function decoding the pulse-width modulation (PWM) bit streams into the non-return-to-zero (NRZ) bit streams

3.18

PWM encoding

PWME

physical coding sublayer (PCS) (3.15) function encoding the non-return-to-zero (NRZ) bit streams into the pulse-width modulation (PWM) bit streams

3.19

receiver

node that, while the *bus* (3.3) is not idle, is neither a *transmitter* (3.23) nor is it integrating

3.20

RXD

port of the *attachment unit interface (AUI)* (3.2) used to transmit the actual state of the physical medium, in binary format, to the *physical coding sublayer (PCS)* (3.15)

3.21

signal improvement capability

SIC

capability to suppress the ringing on the MDI

Note 1 to entry: It is as specified in the high-speed physical medium attachment (HS-PMA) implementation parameter set C in [Table 14](#) and [Table 17](#).

3.22

SIC mode standards.iteh.ai/catalog/standards/iso/1517b356-0680-45f6-a27e-619f8e26ef6e/iso-11898-2-2024 mode according to the high-speed physical medium attachment (HS-PMA) during the arbitration phase

Note 1 to entry: For PMA implementations, it is according to parameter set C or [Annex A](#).

3.23

transmitter

node sending CAN frames

3.24

TXD

port of the *attachment unit interface (AUI)* (3.2) driven by the *physical coding sublayer (PCS)* (3.15) to control how the *physical medium attachment (PMA)* (3.16) influences the actual state of the physical medium

4 Abbreviated terms

For the purposes of this document, the symbols and abbreviated terms given in ISO 11898-1 and the following apply. If the definition of the term in this document is different from the definition in ISO 11898-1, this definition applies.

CAN	controller area network
DLC	data length code
ECU	electronic control unit
EMC	electromagnetic compatibility
ESD	electro static discharge
GND	ground
HS-PMA	high-speed PMA
NRZ	non-return-to-zero
OSI	open layer system
PMD	physical medium dependent
PN	partial networking
PWM	pulse width modulation
RF	radio frequency
WUF	wake-up frame
WUP	wake-up pattern

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5 HS-PMA function

5.1 Base requirements

The HS-PMA comprises one transmitter and one receiving entity. It shall be able to bias the connected physical medium, an electric two-wire cable, relative to a common ground. The transmitter entity shall drive a differential voltage between the CAN_H and CAN_L signals to signal a logical 0 (dominant) or shall not drive a differential voltage to signal a logical 1 (recessive) to be received by other nodes connected to the very same medium. These two signals are the interface to the PMD sublayer.

The HS-PMA shall provide an AUI to the physical coding sublayer as specified in ISO 11898-1. It comprises the TXD and RXD signals as well as the GND signal. The TXD signal receives from the physical coding sublayer the bit stream to be transmitted on the MDI. The RXD signal transmits to the physical coding sublayer the bit stream received from the MDI.

Implementations that comprise one or more HS-PMAs shall at least support the normal-power mode of operation. A low-power mode may be implemented.

Some of the items specified in the following depend on the operation mode of the (part of the) implementation, in which the HS-PMA is included.

[Table 1](#) shows the possible combinations of HS-PMA operating modes and expected behaviour.

Table 1 — HS-PMA operating modes and expected behaviour

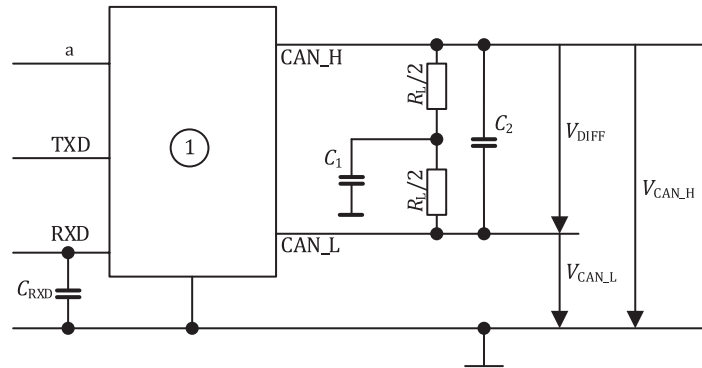
Operating mode	Bus-biasing behaviour	Transmitter behaviour
Normal-power mode	Bus biasing active	Dominant or recessive ^a
Low-power mode	Bus biasing active or inactive	Recessive

^a Depends on input conditions as described in this document.

Parameters given in [Clause 5](#) shall be fulfilled throughout the operating temperature range and supply voltage range (if not explicitly specified for unpowered) as specified individually for every HS-PMA implementation.

5.2 HS-PMA test circuit

The outputs of the HS-PMA implementation to the CAN signals are called CAN_H and CAN_L, TXD is the transmit data input and RXD is the receive data output. [Figure 2](#) shows the external circuit used to measure the specified voltage and current parameters. R_L represents the effective resistive load (bus load) for an HS-PMA implementation, when used in a network, and C_1 represents an optional split-termination capacitor. The values of R_L and C_1 vary for different parameters that the HS-PMA implementation needs to meet and are given as condition in the tables of related parameters.



Key

1 PMA implementation

V_{Diff} differential voltage between CAN_H and CAN_L wires

V_{CAN_H} single-ended voltage on CAN_H wire

V_{CAN_L} single-ended voltage on CAN_L wire

C_{RXD} capacitive load on RXD

C_1 optional split-termination capacitor

C_2 differential capacitive load

R_L differential load resistance

a Power supply for the PMA implementation.

Figure 2 — HS-PMA test circuit

5.3 Static parameter

5.3.1 Maximum ratings of V_{CAN_H} , V_{CAN_L} and V_{Diff}

[Table 2](#) specifies upper and lower limit static voltages, which can be applied to CAN_H and CAN_L without causing damage, while V_{Diff} stays within in its own maximum rating range.

Table 2 — HS-PMA maximum ratings of V_{CAN_H} , V_{CAN_L} and V_{Diff}

Parameter description	Notation	Value	
		Min. [V]	Max. [V]
Maximum rating	V_{Diff}^a	-5,0	+10,0
General maximum rating	V_{CAN_H} , V_{CAN_L}	-27,0	+40,0
Optional: Extended maximum rating	V_{CAN_H} , V_{CAN_L}	-58,0	+58,0
<p>^a This is required regardless whether general or extended maximum rating for V_{CAN_H} and V_{CAN_L} is fulfilled.</p> <p>Applies to HS-PMA implementation powered and unpowered conditions. Applies to transmit data input de-asserted and transmit data input (TXD) becomes asserted while CAN_H or/and CAN_L connected to a fixed voltage.</p> <p>The maximum rating for V_{Diff} excludes that all combinations of V_{CAN_H} and V_{CAN_L} are compliant to this document. $V_{Diff} = V_{CAN_H} - V_{CAN_L}$, see Figure 2.</p>			

5.3.2 Recessive output characteristics, bus biasing active

[Table 3](#) specifies the recessive output characteristics when bus biasing is active.

Table 3 — HS-PMA recessive output characteristics, bus biasing active

Parameter	Notation	Value		
		Min. [V]	Nom. [V]	Max. [V]
Single-ended output voltage on CAN_H ^a	V_{CAN_H}	+2,0	+2,5	+3,0
Single-ended output voltage on CAN_H ^b	$V_{CAN_H_rec}$	+2,137	+2,5	+2,887
Single-ended output voltage on CAN_L ^a	V_{CAN_L}	+2,0	+2,5	+3,0
Single-ended output voltage on CAN_L ^b	$V_{CAN_L_rec}$	+2,137	+2,5	+2,887
Differential output voltage	V_{Diff}	-0,5	0	+0,05
<p>NOTE // The requirements in this table apply concurrently. Therefore, not all combinations of V_{CAN_H} and V_{CAN_L} are compliant with the defined differential output voltage.</p> <p>^a Measurement setup according to Figure 2 (including implementations with selective wake-up function): $R_L > 10^{10} \Omega$ (not present) $C_1 = 0$ pF (not present) $C_2 = 0$ pF (not present) $C_{RXD} = 0$ pF (not present)</p> <p>^b Measurement setup according to Figure 2: $R_L = 60 \Omega$ (tolerance $\leq \pm 1 \%$) $C_1 = 0$ pF (not present) $C_2 = 0$ pF (not present) $C_{RXD} = 0$ pF (not present)</p>				

5.3.3 Recessive output characteristics, bus biasing inactive

[Table 4](#) specifies the recessive output characteristics when bus biasing is inactive.

Table 4 — HS-PMA recessive output characteristics, bus biasing inactive

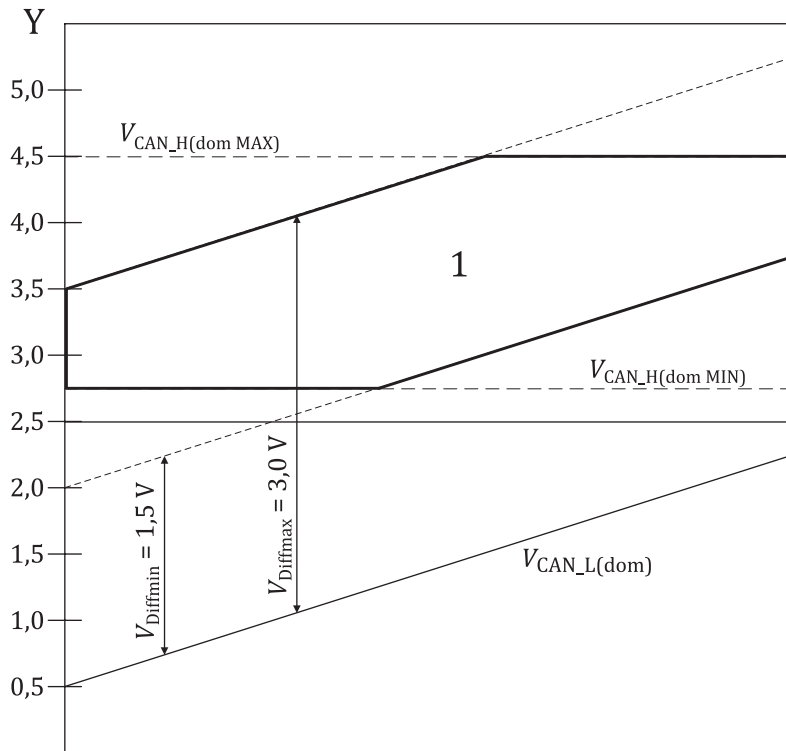
Parameter	Notation	Value ^a		
		Min. [V]	Nom. [V]	Max. [V]
Single-ended output voltage on CAN_H	V_{CAN_H}	-0,1	0	+0,1
Single-ended output voltage on CAN_L	V_{CAN_L}	-0,1	0	+0,1
Differential output voltage	V_{Diff}	-0,2	0	+0,2
NOTE See 5.5.6 to determine when bias is inactive.				
^a Measurement setup according to Figure 2:				
$R_L > 10^{10} \Omega$ (not present)				
$C_1 = 0$ pF (not present)				
$C_2 = 0$ pF (not present)				
$C_{RXD} = 0$ pF (not present)				

5.3.4 Dominant output characteristics

Table 5 specifies the output characteristics during dominant state. Figure 3 illustrates the voltage range for the dominant state.

Table 5 — HS-PMA dominant output characteristics

Parameter	Notation	Value ^a			Condition ^b
		Min. [V]	Nom. [V]	Max. [V]	
Single-ended voltage on CAN_H	V_{CAN_H}	+2,75	+3,5	+4,5	$R_L = 50 \Omega$ to 65Ω
Single-ended voltage on CAN_L	V_{CAN_L}	+0,5	+1,5	+2,25	$R_L = 50 \Omega$ to 65Ω
Differential voltage on normal bus load	V_{Diff}	+1,5	+2,0	+3,0	$R_L = 50 \Omega$ to 65Ω
Differential voltage on effective resistance during arbitration	V_{Diff}	+1,5	Not defined	+5,0	$R_L = 2\ 240 \Omega$ (See NOTE)
Optional: Differential voltage on extended bus load range	V_{Diff}	+1,4	+2,0	+3,3	$R_L = 45 \Omega$ to 70Ω
NOTE Assuming a maximum R_L of 70Ω , this scenario covers a 32-node network ($2\ 240 \Omega / 70 \Omega = 32$), $2\ 240 \Omega$ is emulating a situation with up to 32 nodes transmitting dominant value simultaneously. In such case, the effective load resistance for single nodes decreases (a node does drive only a part of the nominal bus load).					
^a Requirements given in this table apply concurrently. Therefore, not all combinations of V_{CAN_H} and V_{CAN_L} are compliant with the defined differential voltage (see Figure 3).					
^b Measurement setup according to Figure 2:					
$C_1 = 0$ pF (not present)					
$C_2 = 0$ pF (not present)					
$C_{RXD} = 0$ pF (not present)					



Key

- Y V_{CAN_H} and V_{CAN_L}
- 1 range of $V_{CAN_H(dom)}$
- V_{Diff} differential voltage between CAN_H and CAN_L wires
- V_{CAN_H} single-ended voltage on CAN_H wire
- V_{CAN_L} single-ended voltage on CAN_L wire

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Figure 3 — Voltage range of V_{CAN_H} during dominant state of CAN node, when V_{CAN_L} varies from minimum to maximum voltage level (50-Ω to 65-Ω bus-load condition)

<https://standards.iteh.ai/catalog/standards/iso/1517b356-0680-45f6-a27e-619f8e26ef6e/iso-11898-2-2024>

5.3.5 Maximum driver output current

[Table 6](#) specifies the maximum HS-PMA driver output current.

Table 6 — Maximum HS-PMA driver output current

Parameter	Notation	Value ^a		Condition
		Min. [mA]	Max. [mA]	
Absolute current on CAN_H	I_{CAN_H}	not specified	115	$-3\text{ V} \leq V_{CAN_H} \leq +18\text{ V}$
Absolute current on CAN_L	I_{CAN_L}	not specified	115	$-3\text{ V} \leq V_{CAN_L} \leq +18\text{ V}$

NOTE It is expected that the implementation does not stop driving its output dominant when the differential voltage between CAN_H and CAN_L is outside the limits given in the condition column. The minimum output current is implicitly specified in [Table 5](#) and thus can be expected to be above 30 mA.

^a Measurement setup according to [Figure 2](#):

$R_L > 10^{10}\ \Omega$ (not present)

$C_1 = 0\text{ pF}$ (not present)

$C_2 = 0\text{ pF}$ (not present)

$C_{RXD} = 0\text{ pF}$ (not present)