



SLOVENSKI STANDARD
SIST CECC 23 300-801:2002
01-maj-2002

Capability Detail Specification: Multi-layer printed boards

Capability Detail Specification: Multi-layer printed boards

Bauartspezifikation zur Anerkennung der Befähigung: Mehrlagen-Leiterplatten

Spécification particulière d'agrément: Cartes imprimées multicouches

Ta slovenski standard je istoveten z: **CECC 23 300-801:1998**

[SIST CECC 23 300-801:2002](https://standards.iteh.ai/catalog/standards/sist/fbdad080-963f-4234-93ab-84010eb9a79a/sist-cecc-23-300-801-2002)

<https://standards.iteh.ai/catalog/standards/sist/fbdad080-963f-4234-93ab-84010eb9a79a/sist-cecc-23-300-801-2002>

ICS:

31.180 Varnost: Izdelki za tiskane elektronske plošče
Printed circuits and boards

SIST CECC 23 300-801:2002

en

iTeh STANDARD PREVIEW
(standards.iteh.ai)

[SIST CECC 23 300-801:2002](https://standards.iteh.ai/catalog/standards/sist/fbdad080-963f-4234-93ab-84010eb9a79a/sist-cecc-23-300-801-2002)

<https://standards.iteh.ai/catalog/standards/sist/fbdad080-963f-4234-93ab-84010eb9a79a/sist-cecc-23-300-801-2002>

DETAIL SPECIFICATION
SPÉCIFICATION PARTICULIÈRE
BAUARTSPEZIFIKATION

CECC 23 300-801

February 1998

Supersedes EN 123300-800:1992

English version

**Capability Detail Specification:
Multi-layer printed boards**

Spécification particulière
d'Agrément:
Cartes imprimées multicouches

Bauartspezifikation zur Anerkennung der
Befähigung:
Mehrlagen-Leiterplatten

iTeh STANDARD PREVIEW
(standards.iteh.ai)

[SIST CECC 23 300-801:2002](https://standards.iteh.ai/catalog/standards/sist/84010eb9a79a/sist-cecc-23-300-801-2002)

<https://standards.iteh.ai/catalog/standards/sist/84010eb9a79a/sist-cecc-23-300-801-2002>



This CECC Detail Specification was approved on 1997-08-06.

Up-to-date lists and bibliographical references of other detail specifications relating to EN 123000:1991 and EN 123300:1992 may be obtained on application to the Central Secretariat or to any CENELEC member.

This CECC Detail Specification exists in three official versions (English, French, German). A version in any other language made by translation under the responsibility of a CENELEC member into its own language and notified to the Central Secretariat has the same status as the official versions.

CENELEC members are the national electrotechnical committees of Austria, Belgium, Czech Republic, Denmark, Finland, France, Germany, Greece, Iceland, Ireland, Italy, Luxembourg, Netherlands, Norway, Portugal, Spain, Sweden, Switzerland and United Kingdom.

CENELEC

European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

Central Secretariat: rue de Stassart 35, B - 1050 Brussels

Foreword

This Capability Detail Specification has been prepared by CENELEC/TC CECC/SC 52, Printed Boards (formerly designated CECC Working Group 23).

It was approved as CECC 23 300-801 on 1997-08-06.

This Capability Detail Specification replaces EN 123300-800:1992.

It should be read in conjunction with EN 123000:1991 and EN 123300:1992 and with the current regulations for the CECC System.

iTeh STANDARD PREVIEW (standards.iteh.ai)

[SIST CECC 23 300-801:2002](https://standards.iteh.ai/catalog/standards/sist/fbdad080-963f-4234-93ab-84010eb9a79a/sist-cecc-23-300-801-2002)

<https://standards.iteh.ai/catalog/standards/sist/fbdad080-963f-4234-93ab-84010eb9a79a/sist-cecc-23-300-801-2002>



CONTENTS

	Page
1 GENERAL	
1.1 Scope	4
1.2 Object	4
2 CAPABILITY QUALIFYING COMPONENT	
2.1 Materials	4
2.2 Surface finishes	5
2.2.1 Metallic finishes	5
2.2.1.1 Accelerated ageing	5
2.2.2 Organic finishes	5
2.3 Variant designation	5
3 CAPABILITY APPROVAL	
3.1 Range of capability approval	6
3.2 QPL information	6
4 CAPABILITY TEST PROGRAMME	
4.1 Capability demonstration	6
4.1.1 Other metallic surface finishes	6
4.1.2 Organic surface finishes	6
4.1.3 External bonded heatsinks	7
4.1.4 Demonstration of impedance control	7
5 ADDITIONAL CAPABILITY	7
6 TRACEABILITY	7
Table I Capability approval test schedule	8
Table IIa Additional metallic conductor finishes	13
Table IIb Additional contact finishes	16
Table III Permanent organic finishes	17
Table IV Bonded heatsinks	19
Annex A Suitable test pattern for marking inks	21
Annex B Suitable test pattern for solder masks	22
Annex C Suitable test pattern for bonded heatsinks	23
Annex D Edge connector imperfections	24
Annex E CTP subdivision for thermal shock	25
Annex F Circumferential defects in plated-through holes	26
Annex G Determination of characteristic impedance by TDR	27

ITh STANDARD PREVIEW
(standards.iteh.ai)

<https://standards.iteh.ai/catalog/standards/sist/fbdad080-963f-4234-93ab-8401cc05a79a/sist-cecc-23-300-801-2002>

1 General

1.1 Scope

This Capability Detail Specification (CapDS) is based upon EN 123300. It relates to rigid multilayer printed boards, made with materials and surface finishes as specified in clause 2.

1.2 Object

To specify the Capability Qualifying Component (CQC), its characteristics to be tested, the test methods and conditions to be applied and the requirements to be fulfilled for testing basic and extended capability.

2 Capability Qualifying Component (CQC)

Test boards to be used as CQCs for basic capability shall:

- be made from a combination of the materials specified in 2.1 of this CapDS. The construction shall be as given in 8.3 of EN 123300.
- bear the composite test pattern (CTP) specified in 8.2 of EN 123300 (or equivalent CTP), for basic and other metallic finishes. CTPs as specified in 8.2 of EN 123200 (or equivalent CTP) shall be used to demonstrate organic surface finishes and external bonded heat sinks.
- have one of the surface finishes specified by groups 11, 12, 13, 14, 15, 16, or 18 in 2.2 of this CapDS.

Requirements for test boards to be used as modified CQCs for the demonstration of additional capability are detailed in clause 5 of this CapDS.

2.1 Materials

[SIST CECC 23 300-801:2002](https://standards.iteh.ai/catalog/standards/sist/fbdad080-963f-4234-93ab-84010eb9a79a/sist-cecc-23-300-801-2002)

<https://standards.iteh.ai/catalog/standards/sist/fbdad080-963f-4234-93ab-84010eb9a79a/sist-cecc-23-300-801-2002>

Material Group designation	Specification	Base Material		Base material thickness range (mm)	Cu thickness (µm)
		Type	Grade		
A	EN 60249-2-11	Epoxide Woven Glass	General purpose	0,05 0,8	18, 35, 70, 105
	EN 60249-2-12	Epoxide Woven Glass	Defined flammability		
	EN 60249-3-1G	Pre-preg	General purpose	≥ 0,05	n.a.
	EN 60249-3-1GF	Pre-preg	Defined flammability		

2.2 Surface finishes

2.2.1 Metallic finishes

Finish group Designation	Surface finish	Abbreviation for QPL	Remarks
11	Bare copper	Cu	
12	Copper with solderable organic protective coating	Cu(opc)	
13	Copper with oxide	Cu(CuO)	
14	Tin, Tin-Lead	Sn, SnPb	
15	Tin-Lead (fused)	SnPb(f)	
16	Tin-Lead (dipped and levelled)	SnPb(dl)	
17			not assigned
18	Immersion Gold over Electroless Nickel	AuNi(smt)	
19			not assigned
20			not assigned
21	Specimen K 5 µm, gold plated on copper, remainder using finish group 11-17 (see below)	5AuCu	
22	Specimen K 0,7 µm, gold plated on nickel, remainder using finish group 11-17 (see below)	0,7AuNi	
23	Specimen K 2,5 µm, gold plated on copper, remainder using finish group 11-17 (see below)	2,5AuCu	
24	Specimen K 2,5 µm, gold plated on nickel, remainder using finish group 11-17 (see below)	2,5AuNi	

The demonstration of metallic group finishes 21, 22, 23 or 24 shall be combined with a finish from groups 11, 12, 13, 14, 15, 16 or 18. Each claimed combination of metallic finishes shall be tested separately. Selective and non-selective finishes of the same material, where claimed, must be demonstrated separately.

<https://standards.iteh.ai/catalog/standards/sist/fbdad080-963f-4234-93ab-84010eb9a79a/sist-cecc-23-300-801-2002>

2.2.1.1 Accelerated ageing

The ability of finish groups 11, 12, 13, 14, 15, 16 or 18 to solder after extended or adverse storage conditions is demonstrated using accelerated ageing. This test shall be carried out on those finishes where accelerated ageing is claimed. Each finish that has complied with the requirements of the ageing test is highlighted by the inclusion of an asterisk (*) adjacent to that finish in the manufacturers abstract of capability as published in the QPL.

2.2.2 Organic finishes (where claimed)

Finish group designation	Organic finish	Abbreviation for QPL
a	Dry film solder mask	DSM
b	Wet resist solder mask	WSM
c	Liquid photopolymer solder mask	LSM
d	Marking ink	MI
e	Conductive ink	CI

The demonstration of organic finish groups a, b, c or d shall be over a finish from groups 11, 12, 13, 14, 15, 16 or 18. All claimed types of solder resist shall be tested separately.

2.3 Variant designation

The combination of any material group designated in 2.1 and any of the surface finishes designated in 2.2 constitutes a variant. The variant is designated by the combination of both material and finish group designations. e.g. A12(b) or A12/21(c).

3 Capability approval

3.1 Range of capability approval

Capability approval granted on the testing of one variant is valid within the limits specified in 3.7 of EN 123000 for metal clad base material within one group designation, all base material thicknesses and all foil thicknesses of the material in accordance with 2.1 of this CapDS; and all metallic surface finishes within one surface finish group as given in 2.2.1 of this CapDS, that is:

finish group 11	Covers finish group 11 only
finish group 12	Covers finish group 11 and 12
finish group 13	Covers finish group 11 and 13
finish group 14	Covers finish group 11 and 14
finish group 15	Covers finish group 11 and 15
finish group 16	Covers finish group 11 and 16
finish group 18	Covers finish group 18 only
finish group 21	Covers finish group 21 only
finish group 22	Covers finish group 22 and 24
finish group 23	Covers finish group 21 and 23
finish group 24	Covers finish group 24 only

3.2 QPL information

Information for the QPL (published as CECC 00 200) shall be given in accordance with 3.4 of EN 123000, and shall contain the following details relative to the CapDS:

- reference to the CECC Generic Specification EN 123000
- reference to the CECC Sectional Specification EN 123300
- reference to the CECC CapDS CECC 23 300-801
- base material for which approval is granted as given in 2.1 of this CapDS
- the surface finishes for which approval is granted as given in 2.2 of this CapDS
- any additional capability 3.5.3 of EN 123000 refers

4 Capability test programme

NOTE: In all cases the number of failures permitted is zero.

4.1 Capability demonstration

Capability shall be demonstrated using 9 CTPs of one variant from each material group claimed. Testing shall be in accordance with Table I.

4.1.1 Other metallic surface finishes

If claimed, other metallic surface finishes, as designated in 2.2.1 shall be demonstrated by the manufacture and testing of 3 CTPs plus sufficient extra A and H specimens to meet the requirements of Table II. The maximum active board size for the finish shall be demonstrated. See also clause 5.

4.1.2 Organic surface finishes

Each claimed organic surface finish, as designated in 2.2.2, shall be demonstrated by the manufacture and testing of 3 CTPs using the pattern specified in annex A (marking inks) or annex B (solder masks). Testing shall be in accordance with Table III.

4.1.3 External bonded heatsinks

Where claimed, each bonded heatsink and adhesive system shall be demonstrated by the manufacture of three CTPs complying with 8.2 of EN 123200 (pth), since it is anticipated that manufacturers will also claim capability to that CapDS. Testing shall be in accordance with table IV of this CapDS.

4.1.4 Demonstration of impedance control

Special CQCs shall be constructed in accordance with figure G.5, configured as either a 'stripline' or 'microstrip'. Demonstrations shall be made for the following variants, as required and defined by the approved manufacturer:

- each base material type (e.g. woven glass epoxide);
- each impedance geometry (microstrip, stripline);
- each impedance extreme, and a 50 Ω mandatory demonstration;
- conductor width and lateral separation minima;
- each metallic surface finish.

Tolerances at 50 Ω and each impedance extreme shall be claimed prior to demonstration, and achieved.

For each solder resist type and thickness claimed, impedance value derating factors shall be declared.

Impedance control shall be shown on the Capability Approval certificate as a separate annex.

iTeh STANDARD PREVIEW (standards.iteh.ai)

5 Additional capability

Maximum number of layers	For boards with more than six layers; the construction shall be equivalent to that given for six layers with thicknesses and tolerances altered in proportion to the number of layers claimed.
Maximum active board size	see 8.3 of EN 123000
Plated through hole diameters	Specimen C (microsection coupon) of CTP employed <ul style="list-style-type: none"> • minimum drilled hole diameter; use 2,0 mm pads • minimum clearance diameter; use 2,5 mm pads
Maximum aspect ratio	$\frac{\text{nominal base material thickness for maximum number of layers}}{\text{minimum drilled hole diameter}}$
Minimum conductor width and spacing	Specimen F of the CTP to be modified to provide additionally 5 conductors and 4 spacings, each of the claimed minimum. Initial foil thickness of less than 35 μm may be used for this demonstration, but the thickness used shall be declared.
Metallic conductor finishes	Manufacturers are permitted to demonstrate conductor finishes other than those detailed in 2.2.1. The finish shall be demonstrated in accordance with table IIa and detailed in the manufacturer's Capability Manual.

6 Traceability

Traceability of all specimens to the original product shall be maintained. The method used to identify individual test specimens shall not prejudice the test result.

Table I
Capability approval test schedule

(Table I)

Characteristics	Test No. IEC 60326-2	Specimen of Composite Test Pattern	Requirements	Remarks
<u>General examination</u> <u>Visual examination</u> Conformity and identification	1	All CQCs	Pattern, marking, identification, material and finishes shall comply with this CapDS. There shall be no apparent defects. Any identification for traceability purposes shall be verified.	
Appearance and workmanship	1a	All CQCs	The boards shall appear to have been processed in a careful and workmanlike manner, in accordance with good current practice. The base materials, conductors, surface finishes shall be of uniform appearance and free from cracks, burns, pits, nodules and blisters. Metallic surface finishes shall be free from scratches which penetrate to an underlying surface.	
Plated-through holes	1a	All CQCs	Plated-through holes shall be clean and free from inclusions of any sort that could affect component insertion and solderability, Total area of the voids shall not exceed 10% of the total wall area. The largest dimension shall not exceed 25% of the hole circumference in the horizontal plane, and 25% of the thickness of the board in the vertical plane. Plated-through holes shall have no plating voids at the interface of the hole wall and the conductive pattern or internal layer ring. The interface shall be considered to extend into the hole below the surface of the board a distance of 1,5 times the total copper thickness on the surface or to be two times the inner layer thickness at the level of contact ring.	
	1a		There shall be no circumferential cracks of the copper, or circumferential separation of the copper from the wall of the plated- through hole Holes with plating voids shall not exceed 5% of the total number of plated-through holes	see annex F

(Table I)

Characteristics	Test No. IEC 60326-2	Specimen of Composite Test Pattern	Requirements	Remarks
Conductor defects	1b	All CQCs	There shall be no breaks in conductors intended to be continuous. The presence of local defects (e.g. nicks and pinholes) shall not reduce the conductor width by more than 25% The length of the defect shall not be greater than the nominal conductor width.	Where necessary, this shall be verified by dimensional examination using test 2a. Indentations in conductors, other than those in edge board contacts, shall not be a reason for rejection.
Particles between conductors	1b or 1c	All CQCs	There shall be no conductive material bridging conductors shown as intended to be mutually unconnected by the CTP. Residual particles are permissible provided the leakage path is not reduced by more than 20%.	Where necessary, this shall be verified by dimensional examination using test 2a.
Edge connector defects	2a	All specimens K	The surface of edge board contacts within the contact zone shall be smooth, and free from pitting or scratches penetrating the surface finish. Within the contact zone of each contact, there shall be no more than one indentation or bump. (see annex D)	
<u>Dimensional examination</u> Board Dimensions	2	All CQCs	Dimensions and tolerances shall comply with the CQC outline dimensions.	Thickness measurement of the printed board shall exclude the surface finishes
Flatness	12a	All CQCs	The radius of curvature shall not be less than 3000 mm.	
Board thickness in the zone of edge board contacts	2	all specimens K	1,6 mm ± 0,2 mm. (6 to 8 layers only)	Not applicable to boards with more than 8 layers
Holes	2	All CQCs	Hole diameter shall comply with 8.2 of EN 123300, or as claimed, with a tolerance of ± 0,1 mm.	
Misalignment of hole and land	1a 2a	All CQCs	There shall be no breakout from the land perimeter. There shall be no interruption of the junction between the land and the connecting conductor.	
Conductor width	2	All specimens F	Conductor widths greater than or equal to 0,25 mm shall not deviate from nominal values by more than +0,08 mm, -0,05 mm. Nominal conductor widths less than 0,25 mm shall be within the manufacturer's claimed tolerance	Conductor defects and particles between conductors shall be disregarded when evaluating conductor width and spacing - see 'visual inspection'.
Spacing between conductors	2	All specimens F	Nominal conductor spacings of 0,5 mm shall not be less than 0,42 mm. Nominal conductor spacings of 0,25 mm shall not be less than 0,17 mm. Nominal conductor spacings of less than 0,25 mm shall be within the manufacturer's claimed tolerance.	Artwork for CTPs may need etch factor allowance adjustments in order to satisfy these requirements

(Table I)

Characteristics	Test No. IEC 60326-2	Specimen of Composite Test Pattern	Requirements	Remarks
<u>Electrical tests</u> Resistance Change in resistance of plated-through holes, thermal cycling	3c	6 off D	Specimens shall be subjected to 5 immersions @ 260 °C. The increase in resistance between the first and last 25 °C immersion shall not be greater than 10%. The increase in resistance between the first and last 260 °C immersion shall not be greater than 10%. The increase in resistance during any 260 °C immersion shall not be greater than 120%.	Note: Thermal shock may be applied using either method 19a or 19b of IEC 60326-2.
Change in resistance of interconnections	3c	6 off L	Specimens shall be subjected to 5 immersions @ 260 °C. The increase in resistance between the first and last 25 °C immersion shall not be greater than 10%. The increase in resistance between the first and last 260 °C immersion shall not be greater than 10%. The increase in resistance during any 260 °C immersion shall not be greater than 120%.	Note: Thermal shock may be applied using either method 19a or 19b of IEC 60326-2.
<u>Insulation resistance</u> Preconditioning Measurement at 100 Vdc in standard atmospheric conditions Conditioning ; IEC 60068-2-3 Test Ca damp heat steady state, 40 °C / 95%RH Measurement at 500 Vdc in damp heat conditions Surface layers Internal layers Between layers	6 18a 6 6 6a 6b 6c	 3 off E or J 3 off E or J 3 off M	 Not less than 1000 MΩ Not less than 1000 MΩ Not less than 1000 MΩ Not less than 1000 MΩ	Insulation resistance shall be measured before and after environmental conditioning and at elevated temperature Measure while in damp heat @ 0, 10, and 21 days.
<u>Process contamination</u> Preconditioning Conditioning Measurement at 500 Vdc in damp heat conditions Internal short circuits Measurement at 100 Vdc in standard atmospheric conditions	 18a 6a 4a	 3 off E 6 off C (short circuit coupon)	 IEC 60068-2-3 Test Ca; damp heat steady state for 21 days with 60 Vdc applied. (1 mA maximum). Not less than 100 MΩ Not less than 1000 MΩ	 Measure at 0, 10 and 21 days.