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Information technology — Telecommunications and information exchange between systems — High-level iTeh data link control (HDLC) procedures — Frame structure (standards.iteh.ai)

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<u>ISO/IEC 3309:1993</u>

https://standards.iteh.ai/catalog/standards/sist/5c3ae347-4eec-4183-86d0c5c469b224fb/iso-iec-3309-1993

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Foreword

ISO (the International Organization for Standardization) and IEC (the International Electrotechnical Commission) form the specialized system for worldwide standardization. National bodies that are members of ISO or IEC participate in the development of International Standards through technical committees established by the respective organization to deal with particular fields of technical activity. ISO and IEC technical committees collaborate in fields of mutual interest. Other international organizations, governmental and non-governmental, in liaison with ISO and IEC, also take part in the work.

In the field of information technology, ISO and IEC have established a joint technical committee, ISO/IEC JTC 1. Draft International Standards adopted by the joint technical committee are circulated to national bodies for voting. Publication as an International Standard requires approval by at least 75% of the national bodies casting a vote.

International Standard ISO/IEC 3309 was prepared by Joint Technical Committee ISO/IEC JTC 1, Information technology, Subcommittee SC 6, Telecommunications and information exchange between systems.

https://standards.This fifth edition cancels and replaces the fourth edition (ISO/IEC 3309:1991), and incorporates ISO/IEC 3309 amendment 2.

Annex A of this International Standard is for information only.

Introduction

This International Standard is one of a series to be used in the implementation of various applications which utilize synchronous or start/stop transmission facilities.

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Information technology — Telecommunications and information exchange between systems — High-level data link control (HDLC) procedures — Frame structure

1 Scope

This International Standard specifies the frame structure for data communication systems using bit-oriented high-level data link control (HDLC) procedures. It defines the relative positions of the various components of the basic frame and

the bit combination for the frame delimiting sequence (flag).09:1997 The mechanisms used to achieve bit pattern independence/sist/54 (transparency) within the frame are also defined.9 In addition.jec-3304 two frame checking sequences (FCS) are specified; the rules for address field extension are defined; and the addressing conventions available are described.

Control field encodings and formats are defined in other International Standards.

2 Normative references

The following standards contain provisions which, through reference in this text, constitute provisions of this International Standard. At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on this International Standard arc encouraged to investigate the possibility of applying the most recent editions of the standards indicated below. Members of IEC and ISO maintain registers of currently valid International Standards.

ISO/IEC 646:1991, Information technology — ISO 7-bit coded character set for information interchange.

ISO 2382-9: 1984, Data processing — Vocabulary — Part 09: Data communication.

3 Basic frame structure

In HDLC, all transmissions are in frames. The basic frame structure does not include bits inserted for bit-synchronization

(i.e., start or stop elements, see 4.7.2) or bits or octets inserted for transparency (see 4.5).

Each frame consists of the following fields (transmission sequence left to right):

Flag	Address	Control	Information	FCS	Flag
01111110	8 bits	8 bits	*	16 or 32 bits	01111110

* An unspecified number of bits which in some cases may be a multiple of a particular character size; for example, an octet.

where

Flag = flag sequence

Address = data station address field

Control = control field

Information = information field

FCS = frame checking sequence field

Frames containing only control sequences form a special case where there is no information field. The format for these frames shall be

Flag	Address	Control	FCS	Flag
01111110	8 bits	8 bits	16 or 32 bits	01111110

4 Elements of the frame

4.1 Flag sequence

All frames shall start and end with the flag sequence. All data stations which are attached to the data link shall continuously hunt for this sequence. Thus, the flag is used for frame synchronization. A single flag may be used as both the closing flag for one frame and the opening flag for the next frame.

4.2 Address field

In command frames, the address shall identify the data station(s) for which the command is intended. In response frames, the address shall identify the data station from which the response originated.

4.3 Control field

The control field indicates the type of commands or responses, and contains sequence numbers, where appropriate. The control field shall be used

a) to convey a command to the addressed data station(s) to perform a particular operation, or

b) to convey a response to such a command from the addressed data station.

4.4 Information field

Information may be any sequence of bits. In most cases it will be linked to a convenient character structure, for example octets, but, if required, it may be an unspecified number of bits and unrelated to a character structure. the octet. The method of providing and unambiguously identifying the pad bits is not a subject of this International Standard.

4.5 Transparency

4.5.1 Synchronous transmission

The transmitter shall examine the frame content between the two flag sequences including the address, control and FCS fields and shall insert a "0" bit after all sequences of 5 contiguous "1" bits (including the last 5 bits of the FCS) to ensure that a flag sequence is not simulated. The receiver shall examine the frame content and shall discard any "0" bit which directly follows 5 contiguous "1" bits.

4.5.2 Start/stop transmission - basic transparency

Two levels of transparency processing are specified for use with start/stop mode transmission. These are seven-bit data path transparency (SBDPT), specified in subclause 4.5.2.1; and control-octet transparency, specified in subclause 4.5.2.2. Control-octet transparency shall always be performed. SBDPT is an option, use or non-use of which is selected for a given data link by means outside the scope of this International Standard (e.g., a priori knowledge, bilateral agreement, heuristic implementation techniques).

4.5.2.1 Seven-bit data path transparency

For start/stop transmission there shall be eight (8) information bits between the start element and the stop element. If the information field is other than a multiple of 8 bits, the final <u>ISO/T</u>between sender and receiver as a frame-image derived from remainder less than an octet will require pad bits to complete alog/stathand states are as follows, and as indicated in figure 1.

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Figure 1 - Original Frame to Frame-Image Transition

The sequence of octets making up the frame content is considered as divided into a sequence of contiguous sevenoctet segments, with possibly a final segment having length between one and six octets inclusive. These segments are referred to as "original segments."

The frame-image consists of a sequence of image segments defined, in one-to-one correspondence with the original segments, as follows:

a) image segments occur in the same order as the corresponding original segments;

b) each image segment is one octet longer than its original segment;

c) the first part of each image segment is a copy of its original segment, but with the most significant bit (MSB) of each octet set to zero;

d) the remaining, final, octet of each image segment has its least significant bit (LSB) set to the value of the MSB of the last octet of the original segment, its next to least significant bit set to the value of the MSB of the next to last octet (if any) of the original segment, and so on;

e) in the final octet of each image segment, all higher order bits for which no corresponding octet exists in the original segment are set to zero.

NOTE 1 — At the transmitter, the final octet of each image segment can be generated by shifting left the MSB of each octet in the original segment, in sequence, into an initially zero octet: this achieves the correct bit-positioning both for complete seven-octet segments and any short segment at the end of the frame. https://standards.iteh.ai/catalog/standards

NOTE 2 — The MSB of each image-segment octet is defined as zero only for uniqueness of the mapping: because its value is known and plays no part in the reconstruction of the original segment at the receiver, it need not actually be transferred across data paths that, for example, force parity setting of the MSB of each octet.

4.5.2.2 Control-octet transparency

The following transparency mechanism shall be applied to each frame-image: a frame-image is as defined in subclause 4.5.2.1 when SBDPT is selected, and otherwise is identical to the frame content from address field to FCS field inclusive.

The control escape octet is a transparency identifier that identifies an octet occurring within a frame to which the following transparency procedure is applied. The encoding of the control escape octet is:

12345678 Bit position in octet 10111110 Low order bit, first bit transmitted/received

The transmitter shall examine the frame-image between the opening and closing flag sequences including the address,

control, and FCS fields and, following completion of the FCS calculation, shall:

a) Upon the occurrence of the flag or a control escape octet, complement the 6th bit of the octet, and

b) Insert a control escape octet immediately preceding the octet resulting from the above prior to transmission.

The receiver shall examine the frame-image between the two flag octets and shall, upon receipt of a control escape octet and prior to FCS calculation:

a) Discard the control escape octet, and

b) Restore the immediately following octet by complementing its 6th bit.

NOTE — Other octet values may optionally be included in the transparency procedure by the transmitter. Such inclusion shall be subject to prior system/application agreement.

4.5.3 Start/stop transmission - extended transparency

When necessary and by prior agreement between the stations, the transmitter may apply the above transparency procedure (4.5.2) to octets in the groups defined below, in addition to the flag and control escape octets.

4.5.3.1 Flow-control transparency

The flow-control transparency option provides transparency processing for the DC1/XON and DC3/XOFF control characters defined in ISO 646 (i.e., 1000100x and 1100100x, respectively, where "x" may be either "0" or "1"). This has the effect of assuring that the octet stream does not contain values which could be interpreted by intermediate equipment as flow control characters (regardless of parity).

4.5.3.2 Control-character octet transparency

The control-character octet transparency option provides transparency processing for all octets in which both the 6th and 7th bits are "0" (i.e., xxxxx00x, where "x" may be either "0" or "1") as well as for the DELETE character octet (i.e., 1111111x, where "x" may be either "0" or "1"). This has the effect of assuring that the octet stream does not contain values which could be interpreted by intermediate equipment as the control characters or DELETE character defined by ISO 646 (regardless of parity).

4.6 Frame checking sequencing (FCS) field

4.6.1 General

Two frame checking sequences are specified; a 16-bit frame checking sequence and a 32-bit frame checking sequence. The 16-bit frame checking sequence is normally used. The 32-bit frame checking sequence is for use by prior agreement in those cases that need a higher degree of protection than can be provided by the 16-bit frame checking sequence.

NOTES

1. If future applications show that other degrees of protection are needed, different numbers of bits in the FCS will be specified, but they will be an integral number of octets.

2. Explanatory notes on the implementation of the frame checking sequence are given in Annex A.

4.6.2 16-bit frame checking sequence

The 16-bit FCS shall be the ones complement of the sum (modulo 2) of

a) the remainder of

$$x^{k}(x^{15} + x^{14} + x^{13} + x^{12} + x^{11} + x^{10} + x^{9} +$$

$$x^{\circ} + x' + x^{\circ} + x^{3} + x^{4} + x^{3} + x^{2} + x + 1)$$

divided (modulo 2) by the generator polynomial

 $x^{16} + x^{12} + x^5 + 1$

where k is the number of bits in the frame existing between, but not including, the final bit of the opening flag and the first bit of the FCS, excluding start and stop elements (start/stop transmission), and bits (synchronous transmission) and octets (start/stop transmission) inserted for transparency and

b) the remainder of the division (modulo 2) by the generator polynomial

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x^{16} + x^{12} + x^5 + 1
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of the product of x^{16} by the content of the frame dards existing between, but not including, the final bit of the opening flag and the first bit of the FCS,

excluding start and stop elements (start/stop ISO/IEC 3309 transparency. transmission), and bits (synchronous transmission) alog/standards/ 4eec-4183-86d0and octets (start/stop transmission) inserted 5 for 96224 As a typical implementation, at the transmitter, the initial transparency.

As a typical implementation, at the transmitter, the initial content of the register of the device computing the remainder of the division is preset to all ones and is then modified by division by the generator polynomial (as described above) of the address, control and information fields; the ones complement of the resulting remainder is transmitted as the 16-bit FCS.

At the receiver, the initial content of the register of the device computing the remainder is preset to all ones. The final remainder after multiplication by x^{16} and then division (modulo 2) by the generator polynomial

 $x^{16} + x^{12} + x^5 + 1$

of the serial incoming protected bits and the FCS will be

0001 1101 0000 1111 (x^{15} through x^0 , respectively)

in the absence of transmission errors.

4.6.3 32-bit frame checking sequence

The 32-bit FCS shall be ones complements of the sum (modulo 2) of

a) The remainder of

 $x^{k}(x^{31} + x^{30} + x^{29} + x^{28} + x^{27} + x^{26} + x^{25} + x^{24} + x^{26}$ $x^{23} + x^{22} + x^{21} + x^{20} + x^{19} + x^{18} + x^{17} + x^{16} + x^{16} + x^{17} + x^{16} + x^{17} + x^{16} + x^{16} + x^{17} + x^{16} + x^{16} + x^{17} + x^{16} + x^{16} + x^{17} + x^{16} + x^{16} + x^{17} + x^{16} + x^{16} + x^{17} + x^{16} + x^{17} + x^{16} + x^{16} + x^{17} + x^{16} + x^{16} + x^{17} + x^{16} + x^{17} + x^{16} + x^{17} + x^{16} + x^{16} + x^{17} + x^{16} + x^{17} + x^{16} + x^{16} + x^{17} + x^{16} + x$ $x^{15} + x^{14} + x^{13} + x^{12} + x^{11} + x^{10} + x^9 + x^8 + x^{10}$ $x^7 + x^6 + x^5 + x^4 + x^3 + x^2 + x + 1$ divided (modulo 2) by the generator polynomial $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^{10}$ $x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$,

where k is the number of bits in the frame existing between, but not including, the final bit of the opening flag and the first bit of the FCS, excluding start and stop elements (start/stop transmission), and bits (synchronous transmission) and octets (start/stop transmission) inserted for transparency, and

the remainder of the division (modulo 2) by the b) generator polynomial

$$x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^{10}$$

 $x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$

of the product of x^{32} by the content of the frame iTeh STANDA existing between, but not including, the final bit of the opening flag and the first bit of the FCS, excluding start and stop elements (start/stop transmission), and bits (synchronous transmission) and octets (start/stop transmission) inserted for content of the register of the device computing the remainder

of the division is preset to all ones and is then modified by division by the generator polynomial (as described above) of the address, control and information fields; the ones complement of the resulting remainder is transmitted as the 32-bit FCS.

At the receiver, the initial content of the register of the device computing the remainder is preset to all ones. The final remainder after multiplication by x^{32} and then division (modulo 2) by the generator polynomial

$$x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^{10}$$

 $x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$

of the serial incoming protected bits and the FCS will be

1100 0111 0000 0100 1101 1101 0111 1011 $(x^{31} \text{ through } x^0, \text{ respectively})$

in the absence of transmission errors.

4.7 Transmission considerations

4.7.1 Order of bit transmission

Addresses, commands, responses, and sequence numbers shall be transmitted low-order bit first (for example, the first bit of the sequence number that is transmitted shall have the

weight 2°).

The order of transmitting bits within the information field is not specified in this International Standard.

The FCS shall be transmitted to the line commencing with the coefficient of the highest term.

4.7.2 Start/stop transmission

For start/stop transmission, each octet (whether part of the basic frame structure or inserted by the transparency procedure) is delimited by a start element and a stop element. Mark-hold (continuous logical 1 condition) is used to inter-octet time fill if required. Typical octet transmission is as shown in figure 2.

As an example, one method of aborting a frame would be to transmit 8 contiguous "1" bits.

4.9.2 Start/stop transmission

An invalid frame is defined as one that is not properly bounded by two flags or one that is too short (that is, shorter than four octets between flags when using the 16-bit FCS and shorter than six octets between flags when using the 32-bit FCS, excluding octets inserted for transparency), or one in which octet framing is violated (i.e., a "0" bit occurs where a stop element is expected), or one that ends with a control escape-closing flag sequence. Invalid frames shall be ignored.



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Figure 2 - Typical octet transmission Standards.iteh.ai

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4.8 Inter-frame timet fill //standards.iteh.ai/catalog/standards/sist/5:3Extensions/183-86d0-

4.8.1 Synchronous transmission

Inter-frame time fill shall be accomplished by transmitting either contiguous flags or seven to fourteen contiguous "1" bits or a combination of both.

Selection of the inter-frame time fill method depends on systems requirements.

4.8.2 Start/stop transmission

Inter-frame time fill shall be accomplished by transmitting continuous mark-hold condition (logical "1" state) or continuous flags, or a combination of both.

4.9 Invalid frame

4.9.1 Synchronous transmission

An invalid frame is defined as one that is not properly bounded by two flags or one which is too short (that is, shorter than 32 bits between flags when using the 16-bit FCS and shorter than 48 bits between flags when using the 32-bit FCS). Invalid frames shall be ignored. Thus, a frame which ends with an all "1" bit sequence of length equal to or greater than seven bits shall be ignored.

5.1 Extended address field

A single octet address field shall normally be used and all 256 combinations shall be available.

However, by prior agreement, the address field range can be extended by reserving the first transmitted bit (low-order) of each address octet which would then be set to binary zero to indicate that the following octet is an extension of the address field. The format of the extended octet(s) shall be the same as that of the first octet. Thus, the address field may be recursively extended. The last octet of an address field is indicated by setting the low-order bit to binary one.

When extension is used, the presence of a binary "1" in the first transmitted bit of the first address octet indicates that only one address octet is being used. The use of address extension thus restricts the range of single octet addresses to 128.

5.2 Extended control field

The control field may be extended by one or more octets. The extension methods and the bit patterns for the commands and responses are defined in related International Standard(s).