Designation: F 154 – 02

Standard Guide for Identification of Structures and Contaminants Seen on Specular Silicon Surfaces[1]

This standard is issued under the fixed designation F 154; the number immediately following the designation indicates the year of original adoption or, in the case of revision, the year of last revision. A number in parentheses indicates the year of last reapproval. A superscript epsilon (ε) indicates an editorial change since the last revision or reapproval.

1. Scope

1.1 The purpose of this guide is to list, illustrate, and provide reference for various characteristic features and contaminants that are seen on highly specular silicon wafers. Recommended practices for delineation and observation of these artifacts are referenced. The artifacts described in this guide are intended to parallel and support the content of the SEMI M18. These artifacts and common synonyms are arranged alphabetically in Tables 1 and 2 and illustrated in Figs. 1-68.

2. Referenced Documents

2.1 *ASTM Standards:*

F 523 Practice for Unaided Visual Inspection of Polished Silicon Wafer Surfaces[2]

F 1241 Terminology of Silicon Technology[2]

F 1725 Guide for Analysis of Crystallographic Perfection of Silicon Ingots[2]

F 1726 Guide for Analysis of Crystallographic Perfection of Silicon Wafers[2]

F 1727 Practice for Detection of Oxidation Induced Defects in Polished Silicon Wafers[2]

F 1809 Guide for Selection and Use of Etching Solutions to Delineate Structural Defects in Silicon[2]

F 1810 Test Method for Counting Preferentially Etched or Decorated Surface Defects in Silicon Wafers[2]

2.2 *SEMI Standard:*

M18 Format for Silicon Wafer Specification Form for Order Entry[3]

3. Terminology

3.1 Related terminology may be found in Terminology F 1241.

4. Significance and Use

4.1 This guide contains a compilation of the most commonly observed singularly discernible structures on specular silicon surfaces. Ambiguities and uncertainties regarding surface defects may be resolved by reference to this guide. There is close alignment between this guide and common specifications used for the purchase of silicon wafers.

TABLE 1 Wafer Structural Defects[A,B,C]

Defect	Common Synonyms and Acronyms	Illustrating Figures	Relevant ASTM Standard
Dislocation etch pit	Etch Pit, Pit	1-5	F 1725
Epitaxial stacking fault	epi stacking fault, (ESF) Epitaxial Growth Hillock	6-10	F 1726
Lineage	Grain Boundary	11	F 1725
Oxidation induced stacking fault	oxidation stacking fault, (OSF), oxidation induced stacking fault (OISF)	12-18	F 1727 F 1809
Oxide precipitates	bulk micro-defect, (BMD), bulk precipitate	19	F 1727 F 1809
Shallow pits	S-pit, saucer pit	20-21	F 1727 F 1809
Slip	Slip Lines	22-25	F 1725 F 1727 F 1809
Swirl		26-27	F 1725 F 1727 F 1809
Twin	Twin Lamella Twin Line	28-30	F 1725

[A] Magnifications given in the attached illustrations are for an original frame size of 50×50-mm except as noted.

[B] Unless otherwise noted, all attached figures illustrate polished silicon wafer surfaces.

[C] Unless otherwise noted, all attached figures with magnified images were created using interference contrast microscope equipment.

5. Interferences

5.1 Defects, structures, features, or artifacts revealed or enhanced by the referenced methods and exhibited in this guide must be carefully interpreted. Unless utmost care is exercised, the identification of the structure may be ambiguous.

6. Procedure

6.1 Refer to Practices F 523 and F 1727, Guides F 1725, F 1726, and F 1809, and Test Method F 1810.

7. Keywords

7.1 contaminant; defects; dislocation; epitaxial; fracture; preferential etch; scratch; shallow pit; silicon; slip; stacking fault

[1] This guide is under the jurisdiction of Committee F01 on Electronics and is the direct responsibility of Subcommittee F01.06 on Silicon Materials and Process Control.

Current edition approved Jan. 10, 2002. Published March 2002. Originally published as F 154 – 72T. Last previous edition F 154 – 00.

[2] *Annual Book of ASTM Standards*, Vol 10.05.

[3] Available from Semiconductor Equipment and Materials International, 805 E. Middlefield Rd., Mountain View, CA 94043.

TABLE 2 Polished Surface Visual Characteristics

Defect	Common Synonyms and Acronyms	Illustrating Figure	Relevant ASTM Standards
Area contamination	Contamination, foreign matter, residue	31-32	F 523
Crack	Cleavage, fracture	33-38	F 523
Crater	Slurry ring	39	F 523
Crow's feet	Contact damage	40	F 523
Dimple	Depression	41-42	F 523
Dopant striation ring	Striation	43	F 523
Edge chip	Chip	44-47	F 523
Edge crack	Crack	48	F 523
Edge crown		49	F 523
Epitaxial large point defect	large light point defect, (LLPD), spike	50	F 523
Foreign matter	Contamination, residue	51-52	F 523
Groove	Polished over scratch, microscratch	53-54	F 523
Haze		55-56	F 523
Localized light scatterers (particle contamination)	large light scatterers, (LLS)	57-58	F 523
Mound		59	F 523
Orange peel	Roughness	60	F 523
Pits	Air pocket, hole, crystal originated pit, (COP) insufficient polish	61-63	F 523
Saw mark		64	F 523
Scratches	Handling damage	65-67	F 523
Stain		68	F 523

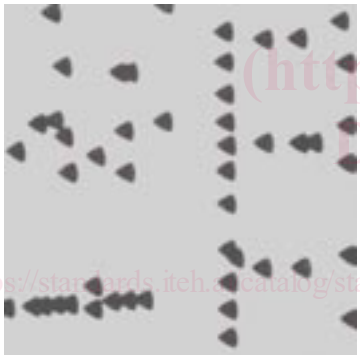

FIG. 1 Dislocation Etch Pits on (111) Silicon, Following 3-Min Sirtl Etch, Magnification 110×.

FIG. 2 Dislocation Etch Pits on (110) Silicon, Following 5-Min Wright Etch, Magnification 110×.

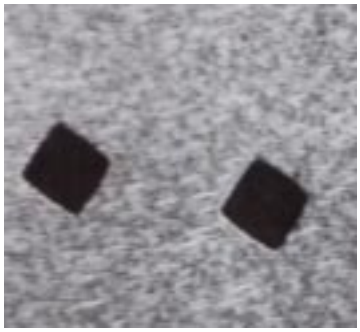

FIG. 3 Dislocation Etch Pits on (100) Silicon Following Schimmel (B) Preferential Etch, Magnification 320×.

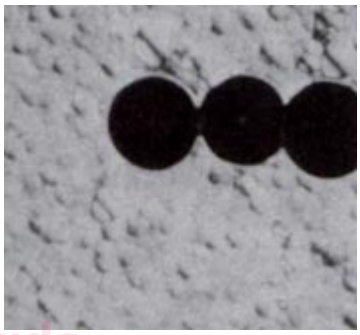

FIG. 4 Dislocation Etch Pits on (100) Silicon Following Sirtl Etch, Magnification 400×.

FIG. 5 Dislocation Etch Pits on (100) Silicon Following 5-Min Wright Etch, Magnification 200×.

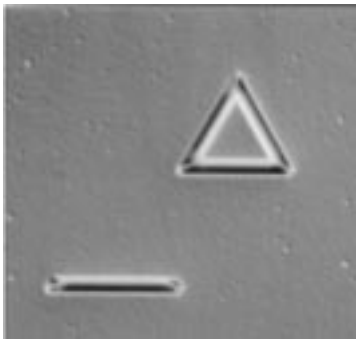

FIG. 6 Epitaxial Stacking Faults on (111), No Preparation Required, Size Dependent Upon EPI Thickness.

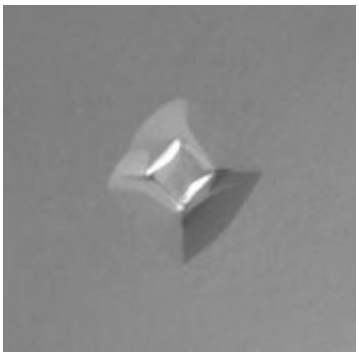

FIG. 7 Epitaxial Stacking Faults on (100), No Preparation Required, Size Dependent Upon EPI Thickness.

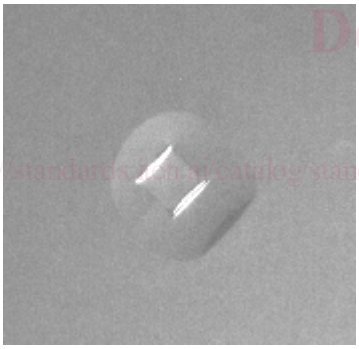

FIG. 8 Epitaxial Stacking Faults on (100), No Preparation Required, Size Dependent Upon EPI Thickness.

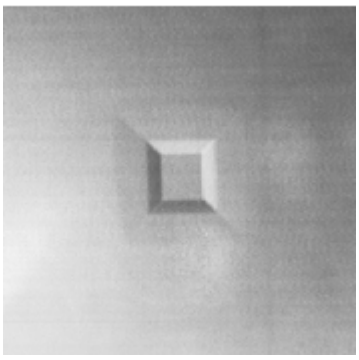

FIG. 9 Epitaxial Growth Hillock on (100), No Preparation Required, Size Dependent Upon EPI Thickness.

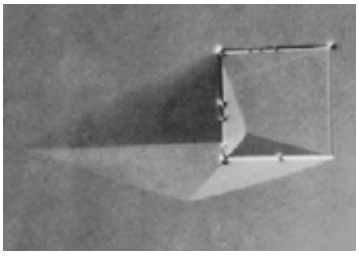

FIG. 10 Epitaxial Stacking Faults on (100), No Preparation Required, Size Dependent Upon EPI Thickness.

FIG. 11 Lineage on (111) Silicon Following Preferential Etch, Magnification 140×.

FIG. 12 Oxidation Induced Stacking Faults on (100) Silicon Following Oxidation and 4-min Wright Etch, Magnification 200×.

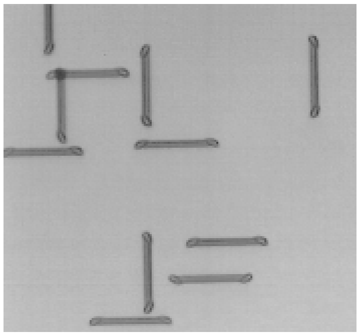

FIG. 13 Oxidation Induced Stacking Faults from Liquid Hone Damage on a (100) Silicon Polished Frontside Surface Following 1100° Oxidation and 1-min Schimmel Etch, Magnification 1500×.

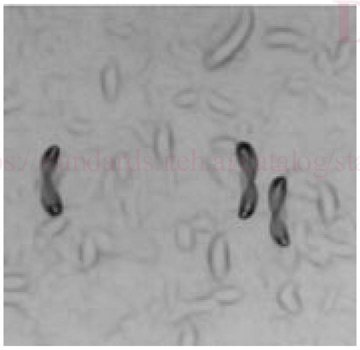

FIG. 14 Oxidation Induced Stacking Faults from Liquid Hone Damage on a (100) Etched Backside Surface Following 1100° Oxidation and 1-Min Schimmel Etch, Magnification 1500×.

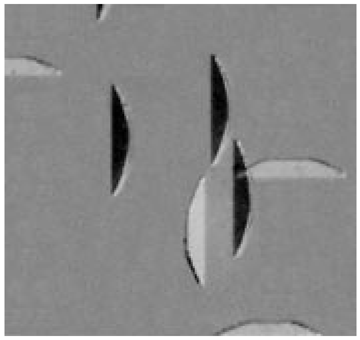

FIG. 15 Oxidation Induced Stacking Faults on (100) Silicon Following Oxidation and 3-Min Secco Etch, Magnification 500×.

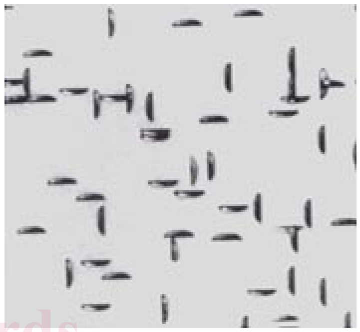

FIG. 16 Oxidation Induced Stacking Faults on (100) Silicon Following Oxidation and 3-min Secco Etch, Magnification 200×.

FIG. 17 Oxidation Induced Stacking Faults on (111) Silicon Following Oxidation and 4 Min Wright Etch, Magnification 200×.

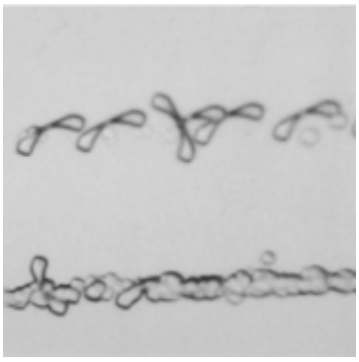

FIG. 18 Oxidation Induced Stacking Faults Caused by a Scratch on (100) Silicon Following Oxidation and 2-min Wright Etch, Magnification 400×.

FIG. 19 Oxidation Induced Stacking Faults and Precipitates Found on the Cleavage Face of a Silicon Wafer After Thermal Treatment and 3-Min Secco Etch, Magnification 100×.

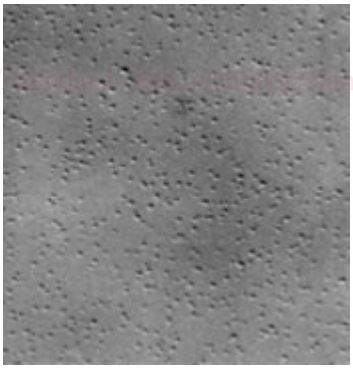

FIG. 20 Relatively Small Shallow Pits on (111) Following Oxidation and 4-Min Wright Etch, Magnification 200×.

FIG. 21 Relatively Large Shallow Pits on (111) Following Oxidation and 4-Min Wright Etch, Magnification 200×.

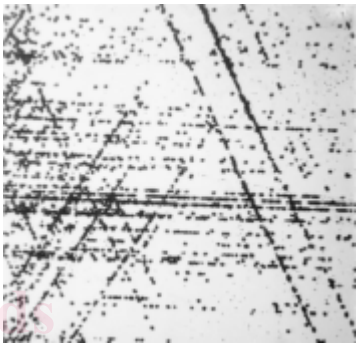

FIG. 22 Slip on a (111) Preferentially Etched Wafer, magnification 5×.

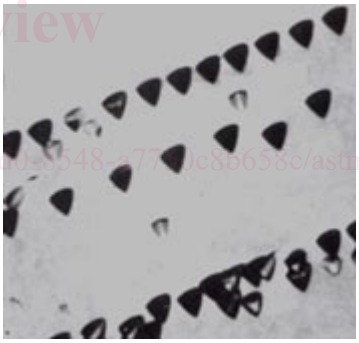

FIG. 23 Slip on a (111) Preferentially Etched Wafer, Magnification 140×.

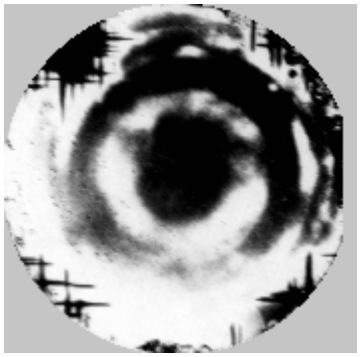

FIG. 24 Slip Lines on a (100) Wafer Visible as a Cross Hatched Pattern Near the Edge Because Shallow Pits are Gettered Following Oxidation and 4-min Wright Etch.

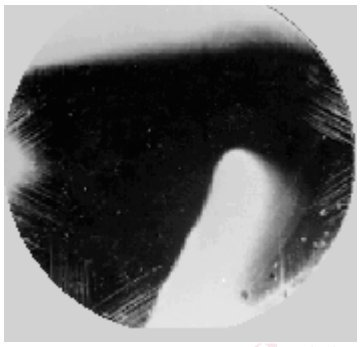

FIG. 25 Slip on a (111) Wafer Following 10-min Wright Etch, Full Wafer View.

FIG. 26 Swirl Pattern Developed by Preferentially Etching a Czochralski Grown 10 to 20 ohm-cm Lapped Silicon Wafer.

FIG. 27 A-swirl on as Grown Float-Zone Silicon Following Preferential Etch, Full Wafer View.

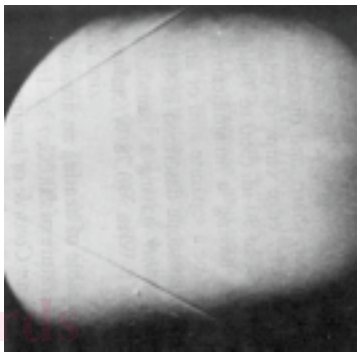

FIG. 28 Twin Lines in a (11) Wafer after Preferential Etching, Full Wafer View.

FIG. 29 Twin Line Following 6.5 micron Epitaxial Deposition, No Other Sample Preparation Required, Magnification 300×.