

INTERNATIONAL STANDARD

IEC
62026-6

First edition
2001-11

Low-voltage switchgear and controlgear – Controller-device interfaces (CDIs) –

Part 6: Seriplex (Serial Multiplexed Control Bus)

*Appareillage à basse tension –
Interfaces appareil de commande-appareil (CDI) –*

*Partie 6:
Seriplex (Serial Multiplexed Control Bus)*

<https://standards.iteh.ai/en/standards/iec/764156ba-9a12-40a5-a6cc-d82bf02f2491/iec-62026-6-2001>

<https://standards.iteh.ai/en/standards/iec/764156ba-9a12-40a5-a6cc-d82bf02f2491/iec-62026-6-2001>



Reference number
IEC 62026-6:2001(E)

As from 1 January 1997 all IEC publications are issued with a designation in the 60000 series. For example, IEC 34-1 is now referred to as IEC 60034-1.

The IEC is now publishing consolidated versions of its publications. For example, edition numbers 1.0, 1.1 and 1.2 refer, respectively, to the base publication, the base publication incorporating amendment 1 and the base publication incorporating amendments 1 and 2.

The technical content of IEC publications is kept under constant review by the IEC, thus ensuring that the content reflects current technology. Information relating to this publication, including its validity, is available in the IEC Catalogue of publications (see below) in addition to new editions, amendments and corrigenda. Information on the subjects under consideration and work in progress undertaken by the technical committee which has prepared this publication, as well as the list of publications issued, is also available from the following:

- Email: custserv@iec.ch
Tel: +41 22 919 02 11
Fax: +41 22 919 03 00

Email: custserv@iec.ch
Tel: +41 22 919 02 11
Fax: +41 22 919 03 00

INTERNATIONAL STANDARD

IEC
62026-6

First edition
2001-11

Low-voltage switchgear and controlgear – Controller-device interfaces (CDIs) –

Part 6: Seriplex (Serial Multiplexed Control Bus)

*Appareillage à basse tension –
Interfaces appareil de commande-appareil (CDI) –*

*Partie 6:
Seriplex (Serial Multiplexed Control Bus)*

<https://standards.iteh.ai/standards/iec/764156ba-9a12-40a5-a6cc-d82bf02f2491/iec-62026-6-2001>

© IEC 2001 — Copyright - all rights reserved

No part of this publication may be reproduced or utilized in any form or by any means, electronic or mechanical, including photocopying and microfilm, without permission in writing from the publisher.

International Electrotechnical Commission
Telefax: +41 22 919 0300

3, rue de Varembé Geneva, Switzerland
e-mail: inmail@iec.ch IEC web site <http://www.iec.ch>



Commission Electrotechnique Internationale
International Electrotechnical Commission
Международная Электротехническая Комиссия

PRICE CODE **XC**

For price, see current catalogue

CONTENTS

FOREWORD.....	4
INTRODUCTION.....	5
1 Scope.....	7
2 Normative references	7
3 Definitions, symbols and abbreviations	8
3.1 Definitions	8
3.2 Symbols and abbreviations.....	13
4 Classification.....	14
4.1 General.....	14
4.2 Frame period, t_f	15
4.3 Signal update time, t_u	15
4.4 Input response time, t_{ir}	16
4.5 Output response time, t_{or}	17
4.6 System response time, t_{sr}	18
5 Characteristics	19
5.1 System overview	19
5.2 Frequency, cable length and node count.....	23
5.3 Data transmission.....	24
5.4 General data transmission features.....	26
5.5 Signal timing.....	31
5.6 Data definitions.....	33
5.7 Signal addressing conventions.....	38
5.8 Operational characteristics.....	39
5.9 Fault responses.....	43
5.10 Device programming.....	48
6 Product information.....	48
7 Normal service, mounting and transport conditions.....	48
7.1 General.....	48
7.2 Ambient air temperature.....	48
7.3 Humidity.....	49
7.4 Conditions during transport and storage	49
7.5 Mounting	49
7.6 Shock.....	49
7.7 Vibration.....	49
8 Constructional and performance requirements.....	49
8.1 Seriplex power supply	49
8.2 Power distribution.....	50
8.3 Isolation	50
8.4 Data line characteristics	51
8.5 Clock line characteristics.....	52
8.6 Seriplex cable topology	54
8.7 Cable specifications	55
8.8 Electromagnetic compatibility	57

9	Tests	59
9.1	Supply polarity	59
9.2	Power supply	59
9.3	Clock source	60
9.4	I/O device	70
9.5	Seriplex cable	81
Figure 1 – Seriplex controller-device interface system diagram		20
Figure 2 – Peer-to-peer timing diagram		21
Figure 3 – Master/slave timing diagram		22
Figure 4 – Example of address multiplexing		22
Figure 5 – Peer-to-peer transmission format		24
Figure 6 – Master/slave mode data transmission format		26
Figure 7 – Sync period diagram		28
Figure 8 – Data signal timing diagram		32
Figure 9 – Check byte formation		37
Figure 10 – Bus Fault Detection pulse		40
Figure 11 – Digital debounce		42
Figure 12 – Data line diagram		51
Figure 13 – Hysteresis		52
Figure 14 – Clock line diagram		53
Figure 15 – Preferred Seriplex topologies		54
Figure 16 – Other controller-device interface topologies		54
Figure 17 – Four-conductor Seriplex cable		56
Figure 18 – Six-conductor Seriplex cable		57
Figure 19 – Circuit for verification of clock source power consumption		60
Figure 20 – Connections for clock signal tests		61
Figure 21 – Clock signal waveform		61
Figure 22 – Test circuit for clock signal		63
Figure 23 – Waveform of clock pulse		64
Figure 24 – Transient current		64
Figure 25 – Test circuit for CDI data signal		65
Figure 26 – Waveform for CDI data signal		65
Figure 27 – Data line waveforms		67
Figure 28 – Connections for verification of data line requirements		68
Figure 29 – Waveforms for verification of data line requirements		68
Figure 30 – Connections for verification of I/O device requirements		71
Figure 31 – Connections for verification of I/O device data line capacitance (a)		71
Figure 32 – Connections for measurement of I/O device data line capacitance (b)		71
Figure 33 – Measurement of I/O device data line capacitance		72
Figure 34 – Connections for measurement of I/O device voltage drop		73

Figure 35 – Connections for measurement of output device lower voltage threshold	73
Figure 36 – Connections for measurement of output device upper voltage threshold.....	74
Figure 37 – Connections for measurement of input device lower voltage threshold	76
Figure 38 – Connections for measurement of input device upper voltage threshold.....	76

Table 1 – Maximum available clock frequency for valid networks (single power supply)	23
Table 2 – Maximum available clock frequency for valid networks (multiple power supplies)...	24
Table 3 – Sync period parameters	28
Table 4 – Symbols and parameters	32
Table 5 – CDR signal address assignments	35
Table 6 – Address codes	36
Table 7 – Channel codes	37
Table 8 – I/O direction codes	37
Table 9 – Seriplex power supply requirements	49
Table 10 – Data line characteristics	51
Table 11 – Clock line characteristics	53
Table 12 – Wire size and characteristics	55
Table 13 – General Seriplex cable characteristics	55
Table 14 – Seriplex cable specifications	56

INTERNATIONAL ELECTROTECHNICAL COMMISSION

**LOW-VOLTAGE SWITCHGEAR AND CONTROLGEAR –
CONTROLLER-DEVICE INTERFACES (CDIs) –****Part 6: Seriplex (Serial Multiplexed Control Bus)**

FOREWORD

- 1) The IEC (International Electrotechnical Commission) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of the IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, the IEC publishes International Standards. Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. The IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
- 2) The formal decisions or agreements of the IEC on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested National Committees.
- 3) The documents produced have the form of recommendations for international use and are published in the form of standards, technical specifications, technical reports or guides and they are accepted by the National Committees in that sense.
- 4) In order to promote international unification, IEC National Committees undertake to apply IEC International Standards transparently to the maximum extent possible in their national and regional standards. Any divergence between the IEC Standard and the corresponding national or regional standard shall be clearly indicated in the latter.
- 5) The IEC provides no marking procedure to indicate its approval and cannot be rendered responsible for any equipment declared to be in conformity with one of its standards.
- 6) Attention is drawn to the possibility that some of the elements of this International Standard may be the subject of patent rights. The IEC shall not be held responsible for identifying any or all such patent rights.

International Standard IEC 62026-6 has been prepared by subcommittee 17B: Low-voltage switchgear and controlgear, of IEC technical committee 17: Switchgear and controlgear.

The text of this standard is based on the following documents:

FDIS	Report on voting
17B/1162/FDIS	17B/1174/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 3.

The committee has decided that the contents of this publication will remain unchanged until 2004. At this date, the publication will be

- reconfirmed;
- withdrawn;
- replaced by a revised edition, or
- amended.

A bilingual version of this publication may be issued at a later date.

INTRODUCTION

The general rules in IEC 62026-1 are applicable to this International Standard, where specifically called for. All such rules, clauses and subclauses, together with tables, figures and annexes, are identified by reference to part 1, for example 7.2.4.1 of IEC 62026-1.

Seriplex (Serial Multiplexed Control Bus) is a controller-device interface which provides a deterministic means of exchanging simple data among control and sensing devices. All devices are connected together by a single shielded four-conductor cable.

Any device which fully conforms to this part of IEC 62026 will be able to perform at least elementary data exchange with other compliant devices through the Seriplex controller-device interface.

Withstand

iTeh Standards
(<https://standards.iteh.ai>)
Document Preview

IEC 62026-6:2001

<https://standards.iteh.ai/en/standards/iec/764156ba-9a12-40a5-a6cc-d82bf02f2491/iec-62026-6-2001>

LOW-VOLTAGE SWITCHGEAR AND CONTROLGEAR – CONTROLLER-DEVICE INTERFACES (CDIs) –

Part 6: Seriplex (Serial Multiplexed Control Bus)

1 Scope

This part of IEC 62026 specifies an interface system between single or multiple controllers, and control circuit devices or switching elements. The interface system uses two twisted conductor pairs within one cable – one of these pairs provides a communication medium and the other pair provides power to the devices. It also establishes requirements for the interchangeability of components with such interfaces.

This standard specifies the physical and operating characteristics of the Seriplex controller-device interface, including:

- requirements for interfaces between controllers and switching elements;
- normal service conditions for devices;
- constructional and performance requirements;
- tests to verify conformance to requirements.

These particular requirements apply in addition to the general requirements of IEC 62026-1.

2 Normative references

The following normative documents contain provisions which, through reference in this text, constitute provisions of this part of IEC 62026. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based on this part of IEC 62026 are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. For undated references, the latest edition of the normative document referred to applies. Members of IEC and ISO maintain registers of currently valid International Standards.

IEC 60068-2-6:1995, *Environmental testing – Part 2: Tests – Test Fc: Vibration (sinusoidal)*

IEC 60068-2-27:1987, *Basic environmental test procedures – Part 2: Tests – Test Ea and guidance: Shock*

IEC 60664-1:1992, *Insulation coordination for equipment within low voltage systems – Part 1: Principles, requirements, and tests*

IEC 60947-1:1999, *Low-voltage switchgear and controlgear – Part 1: General rules*

IEC 61000-4-2:1995, *Electromagnetic compatibility (EMC) – Part 4: Testing and measurement techniques – Section 2: Electrostatic discharge immunity test*. Basic EMC Publication

IEC 61000-4-3:1995, *Electromagnetic compatibility (EMC) – Part 4: Testing and measurement techniques – Section 3: Radiated, radio-frequency, electromagnetic field immunity test*

IEC 61000-4-4:1995, *Electromagnetic compatibility (EMC) – Part 4: Testing and measurement techniques – Section 4: Electrical fast transient/burst immunity test*. Basic EMC Publication

IEC 61000-4-5:1995 *Electromagnetic compatibility (EMC) – Part 4: Testing and measurement techniques – Section 5: Surge immunity test*

IEC 61000-4-6:1996, *Electromagnetic compatibility (EMC) – Part 4: Testing and measurement techniques – Section 6: Immunity to conducted disturbances induced by radio-frequency fields*

IEC 62026-1:2000, *Low-voltage switchgear and controlgear – Controller-device interfaces (CDIs) – Part 1: General rules*

CISPR 11:1997, *Industrial, scientific and medical (ISM) radio-frequency equipment – Electromagnetic disturbance characteristics – Limits and methods of measurement*

3 Definitions, symbols and abbreviations

3.1 Definitions

For the purpose of this of this part of IEC 62026, clause 3 of IEC 62026-1, together with the following additions, apply.

3.1.1

address multiplexing

means of extending the data capacity of a Seriplex controller-device interface by assigning signals to one of 16 multiplex channels and broadcasting the multiplex channel number at the start of each data frame

3.1.2

address sharing

practice of assigning two or more signals to the same address

NOTE In the peer-to-peer mode, all addresses used are typically shared by one input signal and one output signal.

3.1.3

analogue input device

device which converts an external analogue signal to a numeric signal to be transmitted to the controller-device interface as input data

3.1.4

analogue output device

device which converts a Seriplex numeric output signal to an external analogue signal

3.1.5

Bus Fault Detect (BFD) pulse

negative-going (logic high-to-low-to-high) pulse on the data line during the sync period, produced by the clock source, and used by the clock source and I/O devices to evaluate the condition of the Seriplex controller-device interface

3.1.6

bus halt

intentional condition in which generation of the Seriplex clock signal is suspended, so that no data signals are transmitted through the controller-device interface, and all output devices assume their default states

NOTE A bus halt is essentially the same as a clock loss condition; bus halt is usually used to indicate that the condition is normal and intentionally induced by the clock source.

3.1.7**clock**

Seriplex signal which is used to synchronize data exchange among connected devices

3.1.8**clock loss**

condition in which the Seriplex clock signal is not operating due to a fault condition, so that no data signals are transmitted through the controller-device interface, and all output devices assume their default states

3.1.9, t_{clock} **clock loss detection period**

time without a transition of the Seriplex clock signal (low-to-high or high-to-low) after which a device detects a clock loss condition

NOTE Typically, output devices will assume their default states after the clock loss detection period has elapsed.

3.1.10**clock module**

dedicated device which performs clock source functions for a Seriplex CDI operating in peer-to-peer mode

3.1.11**clock pulse**

sequence of logic level transitions on the Seriplex clock line, beginning with a positive (logic low-to-high) transition and including a negative (high-to-low) transition

3.1.12**clock rate**

repetition frequency of the Seriplex clock signal during the data-transmission portion of a data frame

NOTE This rate is the reciprocal of the clock period.

3.1.13**clock source**

Seriplex device which generates the clock signal, provides the current source for the data line, and transmits the Bus Fault Detect pulse

NOTE Usually the clock source is incorporated within an interface to a controller, but for peer-to-peer mode operation this may be a clock module instead.

3.1.14**control software**

software which monitors Seriplex input signals and controls Seriplex output signals

NOTE This software might be C or Basic or other code within a computer, ladder logic within a PLC, or embedded firmware within a dedicated control device. Typically this software performs controller-device interface start/stop functions and interface card initialization as well as signal monitoring and control.

3.1.15**daisy-chain**

method of connecting Seriplex devices by cable segments connected end-to-end

3.1.16**data echo**

feature of Seriplex devices whereby the device receives a signal then retransmits that signal to the controller-device interface

NOTE This feature may be used to indicate to a data-transmission device that a data signal has been properly received by another device.

3.1.17

data frame

sequence of clock pulses on the clock line, bounded at its beginning and end by a sync period

3.1.18

data line capacitance

capacitance of the data line to all the other conductors

3.1.19

data pass-through

interface feature used in master/slave mode, which takes controller-device interface input signals and retransmits them as controller-device interface output signals at the same signal addresses, without the intervention of control software

NOTE This feature mimics peer-to-peer mode operation in that input devices may directly control output devices at the same address without control programming.

3.1.20

default state

state of Seriplex I/O device output signals under initial power-up, clock loss, and bus fault conditions

NOTE Usually this state is the "off" or inactive state, and corresponds to an output signal value of 0.

3.1.21

digital debounce

optional feature of Seriplex devices whereby multiple identical values of a particular discrete controller-device interface output signal are detected in successive data frames in order to cause the Seriplex device to change the logic state of its external output signals

3.1.22

discrete signal

data signal consisting of exactly one bit of information

NOTE Such a signal may assume one of only two states or values—logic high or low, 0 or 1. Both Seriplex input and output data signals and a device's external input and output signals may be discrete signals.

3.1.23

drop

relatively short length of Seriplex cable which is connected to a longer "trunk" cable

NOTE Typically branch lines are 16 m or less, while trunk lines may be hundreds or thousands of metres long.

3.1.24

excess time constant bleedover

effect which occurs when the data line cannot recharge to a high logic state within one-half clock period after being released from a logic low state

NOTE This effect may result in signals with an intended value of 0 being incorrectly interpreted as having a value of 1.

3.1.25

frame length

number of signal addresses transmitted within a single Seriplex data frame

3.1.26

frame period, t_f

time consumed by one data frame, that is, the elapsed time between the end of successive sync periods during normal operation

3.1.27**host interface**

electronic hardware device which allows control software running on a controller to monitor and control I/O devices through a Seriplex controller-device interface by some means such as a backplane interface or controller-device interface gateway

NOTE A host interface typically also provides Seriplex clock source functions.

3.1.28**input propagation delay**

elapsed time between an external input signal event and that signal's availability within a Seriplex input device for transmission to the controller-device interface

3.1.29**input response time, t_{ir}**

a) in **peer-to-peer mode**, elapsed time between an external input signal event and that signal's appearance on the controller-device interface communications medium

b) in **master/slave mode**, the elapsed time between an external input signal event and that signal's availability to a master's internal logic processor

3.1.30**input signal**

signal received by a Seriplex device other than a controller, and reported to the Seriplex controller-device interface

3.1.31**I/O module**

device that converts between Seriplex signals and external signals from control circuit devices

3.1.32**master**

Seriplex device which executes control logic, incorporates the clock source function, has exclusive access to input data, and is the only device which transmits output data

3.1.33**master/slave mode****mode 2**

operating mode comprising a master and one or more slaves

NOTE In this mode, two clock pulses are transmitted per address – one for input data and the other for output data.

3.1.34**multiplex channel number**

integer between 0 and 15 which serves as an extension of the signal address of devices which support address multiplexing

NOTE Each multiplexed signal is assigned to a single multiplex channel, and is transmitted through the Seriplex controller-device interface during data frames in which the multiplex channel number broadcast by the clock source at the beginning of the data frame matches its assigned channel number.

3.1.35**node**

logically active connection to the controller-device interface

NOTE 1 Typical nodes consist of a clock source or I/O devices.

NOTE 2 Passive connections such as T-junctions are not nodes.

3.1.36

numeric signal

group of consecutive input or output data bits which together represent a single number or quantity

NOTE The allowable range of a numeric signal value is determined by the number of bits assigned to that signal, typically 8, 12, or 16, and usually assigned a starting signal address which is a multiple of 16 (0, 16, 32, ..., 240).

3.1.37

output propagation delay, t_{op}

time between a change in the logic state of an output signal within a Seriplex device and the corresponding change in state of its external output signal

3.1.38

output response time, t_{or}

- a) in **peer-to-peer mode**, time between a signal's appearance on the controller-device interface and the corresponding change in state of an external output signal
- b) in **master/slave mode**, elapsed time between a signal's assertion by the controller's internal logic processor (usually into an interface card's memory) and the corresponding change in state of an external output signal

3.1.39

output signal

signal which is received through the controller-device interface by a device other than a controller

3.1.40

peer-to-peer mode

mode 1

operating mode in which one device can control signals to any other device directly, without the intervention of a controller

NOTE In this mode, one clock pulse is transmitted per address, and input and output data are sampled at the same time.

3.1.41

Seriplex device

control or sensing apparatus which is electrically connected to the controller-device interface, including both clock sources and I/O devices

NOTE The term "device" refers collectively to the controller-device interface communications circuitry, to any other circuitry within the device, to any mechanical and/or electromechanical actuators which interface with the device circuitry and to the device's physical housing and electrical connectors.

3.1.42

Seriplex power supply

device which produces the d.c. voltage applied to the controller-device interface circuitry of Seriplex devices

NOTE Typically this power source is electrically isolated from any power sources used to activate control devices or sensors.

3.1.43

signal address

address

integer between 0 and 255 which identifies a single bit of Seriplex input or output data