Designation: F 419 – 94

Standard Test Method for Determining Carrier Density in Silicon Epitaxial Layers by Capacitance-Voltage Measurements on Fabricated Junction or Schottky Diodes [1]

This standard is issued under the fixed designation F 419; the number immediately following the designation indicates the year of original adoption or, in the case of revision, the year of last revision. A number in parentheses indicates the year of last reapproval. A superscript epsilon (ε) indicates an editorial change since the last revision or reapproval.

1. Scope

1.1 This test method covers the measurement of carrier density in silicon epitaxial layers. The precision that can be expected depends upon the carrier-density inhomogeneities parallel and perpendicular to the junction and upon the carrier-density level.

1.2 The measurement requires the formation of Schottky or *p-n* junction diodes on or in the epitaxial layer. In this sense the method is destructive (see, however, 5.2).

1.3 Both *n*- and *p*-type epitaxial layers can be evaluated, on substrates of the same or opposite types, if the layer thickness is greater than twice the zero-bias depletion width plus, for diffused diodes only, the junction depth **(1)**. [2] This test method is also applicable to bulk material.

1.4 This test method covers the carrier density range from about 4×10^{13} to about 8×10^{16} carriers/cm^3 (resistivity range from about 0.1 to about 100 Ω·cm in *n*-type wafers and from about 0.24 to about 330 Ω·cm in *p*-type wafers).

1.5 This test method includes procedures for checking both capacitance- and voltage-measuring equipment.

1.6 This test method provides two means of calculating the carrier density from capacitance-voltage data: an incremental method (12.3.1) and a curve-fitting method (12.3.2).

NOTE 1—An alternative method for determining carrier density in epitaxial layers is given in Test Method F 1392. This and a related method, DIN 50 439, use a mercury-probe Schottky barrier contact rather than a fabricated *p-n* junction or Schottky diode. Therefore, measurements by Test Method F 1392 and DIN 50 439 may not be entirely comparable to those made by this test method. DIN 50 439 is also applicable to gallium arsenide as well as to silicon.

1.7 *This standard does not purport to address all of the safety concerns, if any, associated with its use. It is the responsibility of the user of this standard to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use.* Specific hazard statements are given in 11.8 and 11.14.

2. Referenced Documents

2.1 *ASTM Standards:*

F 95 Test Method for Thickness of Lightly-Doped Silicon Epitaxial Layers on Heavily-Doped Silicon Substrates Using an Infrared Dispersive Spectrophotometer [3]

F 110 Test Method for Thickness of Epitaxial or Diffused Layers in Silicon by the Angle Lapping and Staining Technique [3]

F 723 Practice for Conversion Between Resistivity and Dopant Density for Boron-Doped and Phosphorus-Doped Silicon [3]

F 1392 Test Method for Determining Net Carrier Density Profiles in Silicon Wafers by Capacitance-Voltage Measurements With a Mercury Probe [3]

2.2 *DIN Standard:*

DIN 50 439 Determination of the Dopant Concentration Profile of a Single Crystal Semiconductor Material by Means of the Capacitance-Voltage Method and Mercury Contact [3]

3. Terminology

3.1 *Definitions of Terms Specific to This Standard:*

3.1.1 *breakdown voltage— for the purposes of this test method*, the reverse bias voltage at which the test diode exhibits a leakage current density of 3 mA/cm^2.

4. Summary of Test Method

4.1 The small-signal, high-frequency capacitance of *p-n* junction or Schottky diode is measured as a function of reverse bias voltage. The carrier density as a function of depth is determined from the measured values of capacitance and reverse bias voltage.

5. Significance and Use

5.1 The carrier density is an important material acceptance requirement. In material that is neither too heavily doped nor significantly compensated by impurities of the opposite conductivity type, the resistivity of the epitaxial layer may be determined from the carrier density in accordance with Practice F 723.

[1] This test method is under the jurisdiction of ASTM Committee F-1 on Electronics and is the direct responsibility of Subcommittee F01.06 on Silicon Materials and Process Control.

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[2] The boldface numbers in parentheses refer to the list of references at the end of this test method.

[3] *Annual Book of ASTM Standards*, Vol 10.05.

5.2 This test method is suitable for specification acceptance, process control, and research purposes. Because this test method is destructive, measurements are generally made on a sampling basis unless the test diode to be fabricated is made an integral part of the device into which the wafer is being fabricated.

6. Interferences

6.1 Stray inductance and capacitance, caused by excessive lengths of connecting cable, or improper zeroing of the capacitance bridge or meter can cause significant errors in the capacitance measurement. In homogeneous material, such errors result in the calculation of monotonically increasing or decreasing values of carrier density with distance away from the junction.

6.2 Alternating-frequency test sigals greater than 0.05 V rms can lead to errors in the measured capacitance.

7. Apparatus

7.1 Facilities for fabricating *p-n* junction or Schottky diodes on the test specimen.

7.2 *Capacitance Bridge or Meter*, having ranges from 1 to 1000 pF full scale, or greater, in multiples of 10 or less. The measurement frequency shall be in the range from 0.09 to 1.1 MHz inclusive. The accuracy shall be 1.0 % of full scale or better for each range, and the reproducibility shall be 0.25 % of full scale or better. The instrument shall be capable of sustaining external d-c bias of ±200 V or greater and shall be capable of compensating for an external probe fixture with stray capacitance up to 5 pF or greater. The internal a-c measuring signal shall be 0.05 V rms or less.

7.3 *Digital Voltmeter or Potentiometer*, having a sensitivity of 1 mV or better, an accuracy of 0.5 % of full scale or better, a reproducibility of 0.25 % of full scale or better, an input impedance of 100 MΩ or greater, and a common-mode rejection of 100 dB or greater at 60 Hz.

7.4 *D-C Power Supply*, continuously variable, capable of supplying 0 to ±200 V (open circuit) with a ripple of 1 % of the d-c output or less.

7.5 *Curve Tracer*, capable of monitoring the reverse and forward current-voltage characteristics of the diode. The curve tracer shall be capable of applying 200 V at 0.1 mA in the reverse direction and 1.1 V at 1 mA in the forward direction, and have a sensitivity of 10 µA/division or better.

7.6 *Standard Capacitors* of accuracy 0.25 % or better at the measurement frequency. One capacitor shall be in the range from 1 to 10 pF inclusive and one shall be in the range from 10 to 100 pF inclusive.

7.7 *Precision Voltage Source*, capable of providing output voltages from 0 to 200 V. The accuracy of this source shall be 0.1 % of the output voltage or better.

7.8 *Probe Fixture* that holds the specimens containing the diodes; provides probes for making ohmic contact both to the diffused or barrier region, and to the epitaxial layer; and keeps the diode in the dark during the measurement. Vacuum clamping shall be provided. Contact to the epitaxial layer shall be made either by a front-surface contact or, when the layer and substrate are of the same type, by electrical contact to the substrate by means of the vacuum chuck.

7.9 *Toolmaker's Microscope, Shadowgraph, or Planimeter* capable of measuring the junction diameter to an accuracy of 0.5 % or better or the junction area to an accuracy of 1 % or better.

7.10 *Shielded Cables* for making electrical connections between the probe fixture, power supply, capacitance bridge or meter, and digital voltmeter or potentiometer.

8. Sampling

8.1 Because this test method is destructive (see, however, 5.2), it is not generally practical to measure every wafer in a particular lot. A wafer sampling plan shall therefore be agreed upon between the parties to the test.

8.2 If the specimen preparation (see 9.1) involves the fabrication of an array of diodes on a given wafer, it may not be practical to measure every diode on that wafer. A diode sampling plan shall therefore be agreed upon between the parties to the test.

9. Test Specimen

9.1 Fabricate *p-n* junctions or Schottky diodes on the epitaxial layer using planar or mesa technology (see 11.2).

10. Calibration

10.1 Connect shielded cables of a length suitable for measuring the standard capacitors (see 6.1) to the capacitance bridge or meter. Zero the capacitance bridge or meter with the cables connected to the bridge or meter but not to the standard capacitors.

10.2 Connect the cables to one of the standard capacitors; then measure and record the capacitance in picofarads. Disconnect the capacitor.

10.3 Connect the cables to the other standard capacitor; measure and record the capacitance in picofarads. Disconnect the capacitor.

10.4 To verify that the digital voltmeter or potentiometer is within specification over the range from 1 to 200 V, inclusive, use it to measure the precision voltage source at five or more voltages in that range.

10.5 If either the capacitance- or voltage-measuring equipment is not within the required specifications (see 7.2 and 7.3 for values), make necessary adjustments in accordance with the appropriate instrument instruction manuals to bring equipment to within specifications before proceeding with the measurement of the specimen.

11. Procedure

11.1 Unless the epitaxial layer thickness is already known, measure the epitaxial layer thickness by Test Method F 95 or Test Method F 110, depending on whether the layer and substrate are the same or opposite conductivity type, respectively. Estimate the carrier density in the layer to be measured. Consult Ref **(1)** to determine the depletion region width at zero bias. Double this width to allow for the depletion region widening that will occur when the required reverse biases are applied (see 11.13 and 11.14). If a diffused junction diode is to be fabricated, add the anticipated junction depth to this wider depletion width. Make measurements in accordance with the following procedure only if this wider depletion region width

(plus junction depth if applicable) is less than or equal to the epitaxial layer thickness.

11.2 By means customarily used in microelectronic operations, fabricate several gated or ungated diodes with an active area in the range from 5×10^{-4} to 3×10^{-2} cm^2 inclusive. (For circular active areas this range corresponds to diameters in the range from 0.025 to 0.142 cm (9.9 to 76.8 mils).)

11.2.1 Fabricate junction diodes to have a surface carrier density at least 100 times the carrier density of the epitaxial layer, and a junction depth less than 1.5 µm.

11.3 Measure and record the active device area, in square centimetres, to an accuracy of 1 %, or, if the device is circular, the device diameter, in centimetres, to an accuracy of 0.5 %.

NOTE 2—Refer to Appendix X1 for suggested data sheet formats for recording the data if the data collection and calculations are carried out manually or off-line.

11.4 Transfer the specimen to the probe fixture. Make an electrical connection from the probe fixture to the epitaxial layer as near to the active region as possible. (For epitaxial layers on substrates of the same conductivity type, the connection can be made to the substrate.)

11.5 Make an electrical connection to the barrier or diffused region of the diode by means of a probe. Take care to avoid probe forces high enough to cause the probe to penetrate the diffused layer of shallow diffused diodes and cause shorting or excessive leakage.

11.6 Connect shielded cables from the probe fixture to the curve tracer (see 7.5).

11.7 Measure the diode forward resistance, *R*, in ohms, at 1-V forward bias as follows:

11.7.1 Measure the diode current that exists at 0.9-V forward bias, in milliamperes.

11.7.2 Measure the diode current that exists at 1.1-V forward bias, in milliamperes.

11.7.3 Calculate and record *R* as follows:

$$R = 200/(I_2 - I_1)$$

where:

I_2 = diode current at 1.1-V forward bias, mA, and
I_1 = diode current at 0.9-V forward bias, mA.

11.7.4 Do not proceed with the measurement until a contact of resistance suitably low for the instrument to be used has been achieved. Since values of *R* of 200 Ω or greater can cause measurement error in some capacitance measuring instruments **(2)**, use alloyed, diffused, or metallized contacts as required in order to keep the forward resistance of the specimen below 200 Ω.

11.8 Using the same curve tracer, apply a reverse bias to the test diode and measure and record the breakdown voltage, V_B, in volts (see 3.1). **Caution**—Avoid contact with the probes when bias is applied.

11.9 Reduce the voltage applied to the probe to zero and raise the probe so that electrical contact to the barrier or diffused layer is broken.

11.10 Disconnect the shielded cables from the probe fixture to the curve tracer.

11.11 Connect shielded cables from the probe fixture to the capacitance bridge or meter so that the low side of the bridge or meter is connected to the epitaxial layer or substrate (see 11.4), and the high side of the bridge or meter is connected to the probe that is to contact the barrier or diffused region.

11.12 Zero the capacitance bridge or meter as follows:

11.12.1 With a nominal 1-V reverse bias applied, and with the capacitance bridge or meter set to its least sensitive range, gently lower the probe so that it just makes contact with the barrier or diffused region of the test diode. Detect the point of contact by a positive deflection of the capacitance bridge or meter.

11.12.2 Select the most sensitive range of the capacitance bridge or meter for which the indication does not exceed full scale.

11.12.3 Raise the probe so that electrical contact to the barrier or diffused region is just broken.

11.12.4 Adjust the capacitance bridge or meter so that the indication on the selected range, within the accuracy of the instrument, is 0 pF.

11.13 Lower the probe to contact the barrier or diffused region. Apply a nominal 1-V reverse bias to the test diode and measure the capacitance in picofarads. Record the applied voltage and measured capacitance, each to three or more significant figures, as V_1 and C_1, respectively. Consider the voltages to be positive numbers even though reverse biases are involved.

11.14 Adjust the voltage to obtain a new value of capacitance 4 to 6 % lower than the previous value. Record the voltage and capacitance each to three or more significant figures as V_2 and C_2, respectively. **Caution**—Avoid contact with the probes when bias is applied.

11.15 Repeat 11.14, adjusting the voltage for a 4 to 6 % decrease in capacitance at each step, until either the breakdown voltage is reached or the capacitance values start to increase with increased reverse bias. When the measurement sequence is complete, reduce all biases to zero, raise the probe or probes and remove the specimen from the probe fixture. Use a minimum of four data points for the incremental method (see 12.3.1). For the curve-fitting method (see 12.3.2) use a number of data points consonant with the order of fit expected.

12. Calculations

12.1 If device diameter rather than device area is measured in 11.3, calculate the device area, in square centimetres, as follows:

$$A = 0.7854\, d^2$$

where:

A = area, cm^2, and
d = diameter, cm.

12.2 *Peripheral Correction*—If the diodes to be measured are very small or very deep *p-n* junctions fabricated by diffused planar (as opposed to mesa) technology, a correction for peripheral capacitance may be required. To do this perform the following calculation on each of the measured capacitances, C_i, to subtract the peripheral, or edge, capacitance from the measured capacitance **(3)** and record the results. Otherwise proceed to 12.3.

12.2.1 Calculate and record an estimate of the depletion width, X_0, in centimetres, using the following relation:

$$X_0 = 1.0359\ (A/C_i) \quad (1)$$

where:
A = diode area, cm^2, and
C_i = the ith measured capacitance, pF.

NOTE 3—For measuring materials other than silicon, the right-hand side of Eq 1 must be multiplied by the factor $K/11.7$, where K is the relative dielectric constant of the material under test. The same factor must multiply the right-hand sids of Eq 2, Eq 3, Eq 5, and Eq 6, and the equation for W_i in Eq 8. The reciprocal of the factor multiplies the right-hand side of the equation for N_i in Eq 8 (see Appendix X2 for discussion).

12.2.2 Estimate ith peripheral capacitance, C_{pi}, in picofarads, corresponding to the measured capacitance, C_i, using the appropriate equation in Ref **(3).** For circular, one-sided junctions the following relation is applicable:

$$C_{pi} = \underline{5.7685\sqrt{A}}\,ln\left[\left(1+\frac{X_0}{X_j}\right)/\left(1+\frac{X_0}{0.88623\sqrt{A}+X_j}\right)\right] \quad (2)$$

where:
X_0 = estimate of the depletion width, cm (see 12.2.1),
X_j = junction depth, cm (see 11.2.1) and
A = diode area, cm^2.

12.2.3 Estimate the corrected capacitance, C_{ci}, in picofarads, using the following relation:

$$C_{ci} = C_i - C_{pi}$$

where:
C_i = ith measured capacitance, pF, and
C_{pi} = estimate of the ith peripheral capacitance, pF (see 12.2.2).

12.2.4 Calculate a new estimate of the depletion width, X_1, in centimetres, using the following relation:

$$X_1 = 1.0359(A/C_{ci}) \quad (3)$$

where:
A = diode area, cm^2, and
C_{ci} = estimate of the corrected capacitance, pF (see 12.2.3).

12.2.5 Calculate the relative difference, δ, between the old and new estimates of the depletion width, in centimetres, using the following relation:

$$\delta = (X_1 - X_0)/X_1$$

where:
X_0 = previous estimate of the depletion width, cm (see 12.2.1 or 12.2.6.2), and
X_1 = new estimate of the depletion width, cm (see 12.2.4).

12.2.6 Compare the value of δ with the number 0.0001.

12.2.6.1 If $\delta \leq 0.0001$, record the value of C_{ci} found in 12.2.3 as the corrected value of the capacitance C_i.

12.2.6.2 If $\delta \geq 0.0001$, set $X_0 = X_1$, and calculate and record a new estimate of the depletion width and peripheral capacitance in accordance with 12.2.2 through 12.2.6. Iterate 12.2.2 through 12.2.6 until the condition of 12.2.6.1 is met.

12.3 Calculate the carrier density profile using either the incremental method (12.3.1) or the curve-fitting method (12.3.2).

12.3.1 *Incremental Method* **(4)**:

12.3.1.1 Calculate S_i for i from 1 to $n - 3$, where n is the number of capacitance-voltage data pairs measured above, using the following relation:

$$S_i = \frac{ln\left[\frac{V_{i+3}+0.6}{V_i+0.6}\right]}{\ln\left[\frac{C_i}{C_{i+3}}\right]} \quad (4)$$

where:
V_i = ith recorded voltage, V,
V_{i+3} = $(i + 3)$th recorded voltage, V,
C_i = ith recorded value of capacitance corrected for peripheral capacitance as required (see 12.2), pF, and
C_{i+3} = $(i + 3)$th recorded value of capacitance corrected for peripheral capacitance as required, (see 12.2) pF.

12.3.1.2 Calculate the depth, W_i, in micrometres, corresponding to each capacitance value, C_i, using the following relation:

$$W_i = 10\,359(A/C_i) \quad (5)$$

where:
A = diode area, cm^2, and
C_i = ith recorded value of capacitance corrected for peripheral capacitance as required (see 12.2), pF.

12.3.1.3 Calculate the average depth W_i' for $i = 1$ to $n - 3$ using the following relation:

$$W_i' = \left[\frac{(W_{i+3})^{S_i} - (W_i)S_i}{S_i(W_{i+3} - W_i)}\right]^{\left(\frac{1}{S_i-1}\right)}$$

12.3.1.4 Calculate the carrier density, N_i, corresponding to each averaged depth, W_i', as follows:

$$N_i = 6.466 \times 10^{14}\frac{V_{i+3} - V_i}{W_i'(W_{i+3} - W_i)} \quad (6)$$

12.3.1.5 Calculate the true depth, W'_{ti}, by adding the junction depth to each of the W_i' values.

12.3.2 *Curve-Fitting Method*:

12.3.2.1 Fit a polynomial function having the following form **(5)** to the data:

$$1/C_{fi}^{\ 2} = a_0 + a_1v_i + a_2v_i^{\ 2} + \cdots a_kv_i^{\ k} \quad (7)$$

where:
C_{fi} = ith value of capacitance calculated from the fit, pF,
$a_0 \cdots a_k$ = coefficients with values determined to minimize the expression $(C_i - C_{fi})^{\ 2}$ over all i values, with C_i values corrected as required for peripheral capacitance (see 12.2),
v_i = V_i + 0.600 V, V_i being the ith recorded measurement of voltage, V, and
k = order of the polynomial, chosen so that it represents the lowest-order fit for which $|(C_i - C_{fi})/C_i| \leq 0.01$ for all values of i and for which $k \leq n-1$, where n = number of capacitance-voltage data points taken.

NOTE 4—See Appendix X3 for a subroutine that will fit data with up to a 10th-order polynomial.

12.3.2.2 Calculate the derivative of the polynomial of 12.3.2.1, D_i, using the following relation:

$$D_i = a_1 + 2a_2 v_i + \cdots + k a_k v_i^{k-1}$$

where $a_1 \cdots a_k$, v_i, and k have the same meaning as in (Eq 7) of 12.3.2.1. Erroneous fluctuations in the calculated carrier density may occur if polynomials of order greater than three are used.

12.3.2.3 Calculate the carrier density corresponding to each depletion depth, using the following relations:

$$W_i = 10\,359(A/C_{fi}) \qquad (8)$$
$$N_i = (1.2050 \times 10^{7})/A^2 D_i$$

where:

W_i = depletion depth, µm,
N_i = carrier density, cm^{-3},
A = diode area, cm^2,
C_{fi} = the ith value of capacitance calculated in 12.3.2.1, pF, and
D_i = the ith value of the derivative calculated in 12.3.2.2.

12.3.2.4 Calculate the true depth, W_{ti}, by adding the junction depth to each of the W_i values.

13. Report

13.1 Report the following information:

13.1.1 Operator identification,

13.1.2 Date of measurement,

13.1.3 Lot number, wafer and diode sampling plans, if applicable,

13.1.4 Specimen identification and type,

13.1.5 Diode fabrication process,

13.1.6 Computation method used, and

13.1.7 Calculated carrier density, cm^{-3}, for each depth.

13.2 For referee measurements, also report the following information:

13.2.1 Junction depth for diffused diodes, µm,

13.2.2 Diode forward resistance, Ω, and

13.2.3 Diode area, cm^2.

14. Precision and Bias

14.1 *Precision*—Interlaboratory comparisons have been made to determine the precision of this technique on planar diodes. These junction diodes were fabricated with a 30-mil (0.076 cm) diameter *n*-type diffused layer in a *p*-type epitaxial layer without metallization. The seven *p*-type specimens examined all had {100} surface orientation with a substrate resistivity less than 0.010 Ω-cm. The epitaxial layer carrier densities ranged from approximately 8×10^{14} holes/cm^3 to 2×10^{16} holes/cm^3. On samples with carrier densities less than 1×10^{16} holes/cm^3, three depths were designated by the coordinating lab at which to make measurements. These depths were selected to be at relatively flat portions of the in-depth profile. This same criterion was applied to two depths on the two samples with carrier densities greater than 1×10^{16} holes/cm^3.

NOTE 5—This experiment was conducted using an earlier version of the test method that employed a value of 11.75 for the silicon dielectric constant; this small difference in dielectric constant does not affect the observed variability.

14.2 *Repeatability (Single Laboratory)*— In 90 % of the cases the measurements had a repeatability of <13.7 % (R2S) based on the analysis of data from eight laboratories where seven specimens were measured at the same laboratory on each of three days. The overall range of observed repeatability extended from 0.00 to 44.07 % (R2S). Values of repeatability greater than 15 % can be indicative of a problem in making the measurements. The repeatability data showed a dependence on laboratory, or instrument, as evidenced by the repeatability of the measurements of laboratories 3, 4, and 6 when contrasted to those of laboratories 1, 2, 5, 7, and 8. The repeatability data is tabulated in Table X4.1.

14.3 *Reproducibility (Multilaboratory)*— Based on analysis including eight laboratories and seven specimens measured at each laboratory on each of three days, the precision (R2S) ranged from 7.2 to 22.2 %. Although the comparison was made using diodes fabricated in *p*-type epitaxial layers, there are no reasons to believe measurements made using *n*-type epitaxial layers would have a lower precision. The statistical data is summarized in Table X4.2.

14.4 *Model Data Analysis*—In the case of six laboratories, model capacitance-voltage pairs, were input in the programs used to calculate carrier densities. The carrier densities calculated using the model data are summarized in Table X4.3. The reproducibility (R2S) of these calculated values ranged from 0.0 to 27.8 %. The measured diode values are summarized in Table X4.4 for the same six laboratories that processed the model data. The reproducibility (R2S) of these measured values ranged from 5.2 to 20.8 %. The carrier density calculated from the model data generally exhibited the same level of reproducibility as that of the carrier density measured from diode structures. This result indicates that the multilaboratory reproducibility is biased by the coding used to calculate the carrier density. Table X4.5 lists the model data input and resulting output. The input data are the same as were used in the interlaboratory experiment, but the output data have been calculated using a dielectric constant of 11.7 for silicon in order to facilitate comparisons by users of this test method.

14.5 *Bias*—No information can be presented on the bias of the procedure in this test method for measuring carrier density because no material having an accepted reference value is available.

15. Keywords

15.1 capacitance-voltage method; carrier density; epitaxial wafer; junction diode; polished wafer; resistivity; Schottky diode; silicon; single crystal silicon

APPENDIXES

(Nonmandatory Information)

X1. SAMPLE DATA SHEETS

X1.1 The following are examples of data sheet formats for manual collection and manual or off-line analysis of C-V data. Fig. X1.1 is for data to be analyzed by the Incremental Method and Fig. X1.2 is for data to be analyzed by the Curve-Fitting Method. The data listed must be stored in a format such that it can be retrieved if the system employed performs the calculations internally.

Operator _____ Lot Number _____
Date _____ Sampling Plans _____
Specimen ID _____
Conductivity Type _____

Diode Fabrication Process _____ Junction depth, μm _____
_____ Diode Area, cm^2 _____
_____ Forward Resistance, Ω _____

C_i, pF	C_{ci}, pF	V_i, V	S_i	W_i, μm	W_i', μm	N_i, cm^{-3}	W_{ti}', μm
C_1	C_{c1}	V_1	S_1	W_1	W'_1	N_1	$W_{t1'}$
C_2	C_{c2}	V_2	S_2	W_2	W'_2	N_2	$W_{t2'}$
C_3	C_{c3}	V_3	S_3	W_3	W'_3	N_3	$W_{t3'}$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
C_{n-3}	C_{cn-3}	V_{n-3}	S_{n-3}	W_{n-3}	$W'_{n-3'}$	N_{n-3}	$W_{tn-3'}$
C_{n-2}	C_{cn-2}	V_{n-2}		W_{n-2}			
C_{n-1}	C_{cn-1}	V_{n-1}		W_{n-1}			
C_n	C_{cn}	V_n		W_n			

FIG. X1.1 Example of Data Sheet Format for Capacitance-Voltage Data and Calculations Using the Incremental Method

Operator _____ Lot Number _____
Date _____ Sampling Plans _____
Specimen ID _____
Conductivity Type _____

Diode Fabrication Process _____ Junction depth, μm _____
_____ Diode Area, cm^2 _____
_____ Forward Resistance, Ω _____
Fitting Coefficients: a_1 _____ a_2 _____ a_3 _____ · · · a_k _____

C_i, pF	C_{ci}, pF	V_i, V	C_{fi}, pF	D_i, μm	W_i, μm	N_i, cm^{-3}	W_{ti}, μm
C_1	C_{c1}	V_1	C_{f1}	D_1	W'_1	N_1	W_{t1}
C_2	C_{c2}	V_2	C_{f2}	D_2	W'_2	N_2	W_{t2}
C_3	C_{c3}	V_3	C_{f3}	D_3	W'_3	N_3	W_{t3}
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
C_{n-3}	C_{cn-3}	V_{n-3}	C_{fn-3}	D_{n-3}	W_{n-3}	N_{n-3}	W_{tn-3}
C_{n-2}	C_{cn-2}	V_{n-2}	C_{fn-2}	D_{n-2}	W_{n-2}	N_{n-2}	W_{tn-2}
C_{n-1}	C_{cn-1}	V_{n-1}	C_{fn-1}	D_{n-1}	W_{n-1}	N_{n-1}	W_{tn-1}
C_n	C_{cn}	V_n	C_{fn}	D_n	W_n	N_n	W_{tn}

FIG. X1.2 Example of Data Sheet Format for Capacitance-Voltage Data and Calculations Using the Curve-Fitting Method

X2. NUMERICAL CONSTANTS

X2.1 The numerical constants given in the equations in this test method are lumped constants. This appendix provides details as to the composition of these lumped constants and the values of the individual constants used in deriving them. Table X2.1 gives the lumped constants, their formulas, and the values in both the present and previous editions of this test method. The units in this table include any necessary unit conversions. If there is no entry for a given equation, either there is no lumped constant in the equation or the constant is strictly numeric (for example, as for unit conversion). Table X2.2 gives the values of the individual constants used in this test method. The difference in values between the 1988 and 1994 editions of this test method is in the value of K_{Si}; this was assigned the value 11.75 in the 1988 and earlier editions of this test method, but the generally accepted value is 11.7. The built-in potential, ϕ, may vary from about 0.5 to about 0.8 V; the constant value assumed is an approximation to this parameter.

TABLE X2.1 Lumped Constants Used in Equations in This Test Method

Equation	Formula	Value in 1988 and earlier editions [A]	Value in this edition [A]
(1), (3)	$K_{Si}\epsilon_0$	1.0404 [pF/cm]	1.0359 [pF/cm]
(2)	$K_{Si}\epsilon_0\pi^{3/2}$	5.7931 [pF/cm]	5.7685 [pF/cm]
(2)	$\pi^{1/2}/2$	3.5449/4	0.88623
(4)	θ	0.6 [V]	0.6 [V]
(5), (8)	$K_{Si}\epsilon_0$	10 404 [pF·μm/cm^2]	10 359 [pF·μm/cm^2]
(6)	$K_{Si}\epsilon_0/q$	6.493×10^{14}[(F·μm^2)/(C·cm^3)]	6.466×10^{14}[(F·μm^2)/(C·cm^3)]
(8)	$2/K_{Si}\epsilon_0 q$	1.19985×10^{7}[(cm·F)/(C·pF^2)]	1.2050×10^{7}[(cm·F)/(C·pF^2)]

[A] Note that the units are given in brackets; the symbol C indicates coulombs and the symbol F indicates farads.