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AMERICAN SOCIETY FOR TESTING AND MATERIALS
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Standard Practice for Unaided Visual Inspection of Polished Silicon Wafer Surfaces[1]

This standard is issued under the fixed designation F 523; the number immediately following the designation indicates the year of original adoption or, in the case of revision, the year of last revision. A number in parentheses indicates the year of last reapproval. A superscript epsilon (ε) indicates an editorial change since the last revision or reapproval.

1. Scope

1.1 This practice covers an inspection procedure for determining the surface quality of silicon wafers that have been polished on one side.

1.2 This practice is intended as a large-volume acceptance method and as such does not require use of a microscope or other optical instruments. Because the inspection relies on the visual acuity of the operator, test results may be very operator-sensitive.

NOTE 1—For clarification of the identification of certain observed defects, procedures given in Practices F 154 may be employed.

1.3 Defects visible to the unaided eye on polished wafer surfaces are categorized in three groups by the illumination geometry which best delineates them: front-surface high-intensity light, front-surface diffuse light, and back-surface diffuse light. These defects originate from two sources: (*1*) those which are caused by imperfections in the silicon crystal, and (*2*) those related to the manufacturing process, including handling and packaging.

1.4 The inspection described generally takes place after polishing and post-polish cleaning but before packaging. Although cleaning and packaging procedures are not a part of this practice, the inspection may be performed on a packaged product to determine the effect of such procedures on the quality of the polished wafers.

1.5 The values stated in SI units are to be regarded as the standard. The values given in parentheses are for information only.

1.6 *This standard does not purport to address all of the safety concerns, if any, associated with its use. It is the responsibility of the user of this standard to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use.*

2. Referenced Documents

2.1 *ASTM Standards:*

F 154 Practices and Nomenclature for Identification of Structures and Contaminants Seen on Specular Silicon Surfaces [2]

F 416 Test Method for Detection of Oxidation Induced Defects in Polished Silicon Wafers [2]

2.2 *Federal Standard:*

Fed. Std. No. 209D Clean Room and Work Station Requirements, Controlled Environment [3]

2.3 *Military Standard:*

MIL-STD-105E Sampling Procedures and Tables for Inspection by Attributes [3]

3. Terminology

3.1 *Definitions:*

3.1.1 *back surface—of a semiconductor wafer*, the exposed surface opposite to that upon which active semiconductor devices have been or will be fabricated.

3.1.2 *chip—in semiconductor wafers*, region where material has been removed from the surface or edge of the wafer.

3.1.3 *contaminant, area*—foreign matter that is visible to the unaided eye under high-intensity illumination on the wafer, of extent greater than a single light-point defect.

3.1.4 *crack*—cleavage or fracture that extends to the surface of a wafer.

3.1.5 *cratering*—a surface texture of irregular closed ridges with smooth central regions.

3.1.6 *crow's foot— on semiconductor wafers*, intersecting cracks in a pattern resembling a ''crow's foot'' (*Y*) on {111} surfaces and a cross (+) on {100} surfaces.

3.1.7 *dimple—on semiconductor wafers*, a smooth surface depression larger than 3 mm in diameter.

3.1.8 *front surface—of a semiconductor wafer*, the exposed surface on which active devices have been or will be fabricated.

3.1.9 *groove—in a semiconductor wafer*, a shallow scratch with rounded edges, that is usually the remnant of a scratch not completely removed by mechanical polishing.

3.1.10 *haze—on a semiconductor wafer*, a cloudy or hazy appearance attributable to light scattering by concentrations of microscopic surface irregularities such as pits, mounds, small ridges or scratches, particles, etc.

[1] This practice is under the jurisdiction of ASTM Committee F-1 on Electronics and is the direct responsibility of Subcommittee F01.06 on Electrical and Optical Measurement.

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[2] *Annual Book of ASTM Standards*, Vol. 10.05.

[3] Available from Standardization Documents Order Desk, Bldg. 4 Section D, 700 Robbins Ave., Philadelphia, PA 19111-5094, Attn: NPODS.

3.1.10.1 *Discussion*—The light reflection from an individual irregularity cannot be readily detected by the unaided eye so haze is a mass effect seen as a high density of tiny reflections.

3.1.11 *imbedded abrasive grains—on a semiconductor wafer*, abrasive particles mechanically forced into the surface.

3.1.12 light point defect—an isolated, localized effect on or in a wafer surface such as a particle or pit resulting in increased light scattering intensity relative to the surrounding surface.

3.1.13 *mound—on a semiconductor wafer surface*, irregularly shaped projection with one or more irregularly developed facets.

3.1.14 *orange peel— on a semiconductor wafer surface*, large-featured, roughened type of surface visible to the unaided eye.

3.1.15 *oxide defect*—an area of missing oxide on the back side of back-sealed wafers discernible to the unaided eye.

3.1.16 *pit—on a semiconductor wafer*, a depression in the surface where sloped sides of the depression meet the wafer surface in a distinguishable manner in contrast to the sides of a dimple which are rounded.

3.1.17 *saw exit mark*—a ragged edge at the periphery of the wafer consisting of numerous small adjoining edge chips resulting from saw blade exit.

3.1.18 *saw marks*—surface irregularities in the form of a series of alternating ridges and depressions in arcs whose radii are the same as those of the saw blade used for slicing.

3.1.19 *striations, n—in semiconductor technology*, helical features on the surface of a silicon wafer associated with local variations in impurity concentration.

3.1.19.1 *Discussion*—Such variations are ascribed to periodic dopant-incorporation differences occurring at the rotating solid-liquid interface during crystal growth. These features are visible to the unaided eye after preferential etching and appear to be continuous under 100× magnification.

NOTE 2—Further discussion of striations may be found in Test Method F 416.

3.2 Other defect-related terminology, together with illustrations of defects, may be found in Practices F 154.

4. Summary of Practice

4.1 The polished surface is first illuminated with a high-intensity source of light positioned so that the light beam is normal to the surface. With the background illumination at a specified low level, the surface is observed at an oblique angle. Under this viewing condition, defects that act as light-scattering points are detected.

4.2 Next, the polished surface is illuminated with a large-area diffuse light source. With the same low level of background illumination, the surface is again observed at an oblique angle. Under this viewing condition, defects larger than those observable under intense collimated light are detected.

4.3 Finally, the wafer is turned over and the back side inspected for the presence of large-area defects with the surface illuminated by the large-area diffuse source.

4.4 Identification of the specimen and the presence of defects are recorded.

5. Significance and Use

5.1 Large volumes of polished silicon wafers are produced by the semiconductor industry for daily consumption in the production of various devices. Surface defects are frequently deleterious to device properties.

5.2 The defects described in this practice are visible to the unaided eye under proper lighting conditions, and the inspections are common to most consumers and producers. Therefore, it is important that a uniform inspection technique be used to aid in the manufacture of standard-quality polished silicon wafers.

6. Interferences

6.1 The polished front surface of a silicon wafer can be damaged by any one of a multitude of types of particulate matter normally occurring in the environment. After cleaning, polished wafers must be kept in a clean room or clean-air environment at all times prior to being sealed in packaging. Failure to do this can compromise the quality of a polished wafer.

6.2 The operator in many instances is the most common source of added contamination to the wafer. Coughing, sneezing or even talking can be the source of additional contaminants. Effort must be taken to minimize the operator induced contamination through rigorous clean room practice.

6.3 Tweezers may introduce defects into the polished wafer surface and therefore are not suitable for use with this method.

NOTE 3—The recommended handling method is by means of a manually vacuum pencil (see 7.5) or a robotic pickup tool. Both techniques will be referred to as the pickup device in this practice.

NOTE 4—**Caution:** During the front-surface inspection using intense light, any light reflected by the specimen or surroundings that is permitted to enter the operator's eyes will greatly reduce the operator's visual acuity and effectiveness of inspection and may cause injury to the eye.

6.4 Improper cleaning and packaging methods following this inspection can compromise otherwise acceptable polished wafers.

NOTE 5—It is suggested that the supplier periodically sample his packaged product to determine that packaging is not degrading the polished slices.

7. Apparatus

7.1 *High-intensity Light Source*— quartz halogen lamp with collimated beam intensity greater than 230 klx (22 000 fc).

NOTE 6—Some standard 35-mm slide projectors meet these requirements. [4]

7.2 *Clean-Air Hood* located in a clean room environment consistent with the particle levels being inspected on the wafers. The inspection area should have an ambient light level of 50 to 650 lx (5 to 60 fc) 230 mm (9 in.) from the front edge of the hood.

[4] A slide projector system with F/2.8, 127 mm lens and 300 W quartz halogen lamp is well suited for this application. The beam is not collimated, but has a very long focal length approximating collimation. The projector cooling fan must be properly exhausted from the particle free inspection area.