Designation: F 615M – 95

METRIC

Standard Practice for Determining Safe Current Pulse-Operating Regions for Metallization on Semiconductor Components [Metric][1]

This standard is issued under the fixed designation F 615M; the number immediately following the designation indicates the year of original adoption or, in the case of revision, the year of last revision. A number in parentheses indicates the year of last reapproval. A superscript epsilon (ε) indicates an editorial change since the last revision or reapproval.

1. Scope

1.1 This practice covers procedures for determining operating regions that are safe from metallization burnout induced by current pulses of less than 1-s duration.

NOTE 1—In this practice, "metallization" refers to metallic layers on semiconductor components such as interconnect patterns on integrated circuits. The principles of the practice may, however, be extended to nearly any current-carrying path. The term "burnout" refers to either fusing or vaporization.

1.2 This practice is based on the application of unipolar rectangular current test pulses. An extrapolation technique is specified for mapping safe operating regions in the pulse-amplitude versus pulse-duration plane. A procedure is provided in Appendix X2 to relate safe operating regions established from rectangular pulse data to safe operating regions for arbitrary pulse shapes.

1.3 This practice is not intended to apply to metallization damage mechanisms other than fusing or vaporization induced by current pulses and, in particular, is not intended to apply to long-term mechanisms, such as metal migration.

1.4 This practice is not intended to determine the nature of any defect causing failure.

1.5 *This standard does not purport to address all of the safety concerns, if any, associated with its use. It is the responsibility of the user of this standard to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use.*

2. Terminology

2.1 *Definitions of Terms Specific to This Standard:*

2.1.1 *failure*—a change in the measured resistance of ±10 % $\Delta R/R$ or as agreed upon by the parties to the test.

3. Summary of Practice

3.1 Specimens are selected from the population being evaluated.

3.2 The d-c resistance of each specimen is measured.

3.3 Each specimen is subjected to stress from rectangular current pulses varying in amplitude and duration according to a predetermined schedule of pulse width and amplitudes.

3.4 A second d-c resistance measurement is made on each specimen after each pulse, and it is characterized as having failed or survived.

3.5 The number, *x*, of specimens surviving and the total number, *n*, of specimens tested at each pulse width and amplitude are analyzed statistically to determine the burnout level at each test pulse width for the desired burnout survival probability and confidence level.

3.6 A point corresponding to the burnout level (at the desired probability and confidence level) is plotted for each of the test pulse duration values in the pulse-amplitude, pulse-duration plane. Based on these points, an extrapolation technique is used to plot the boundary of the safe operating region.

3.7 The following items are not specified by the practice and are subject to agreement by the parties to the test:

3.7.1 The procedure by which the specimens are to be selected.

3.7.2 Test patterns that will be representative of adjacent metallization on a die or wafer (5.3).

3.7.3 The schedule of pulse amplitudes and durations to be applied to the test samples (9.8).

3.7.4 The level of probability and confidence to be used in calculations to establish the boundary of the safe operating region (10.1).

3.7.5 The amount of change of resistance that will define the criterion for failure.

3.7.6 The statistical model to be used to determine the burnout probability at a desired stress level.

3.7.7 The form and content of the report.

[1] This practice is under the jurisdiction of ASTM Committee F01 on Electronics and is the direct responsibility of Subcommittee F01.11 on Quality and Hardness Assurance.

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4. Significance and Use

4.1 Solid-state electronic devices subjected to stresses from excessive current pulses sometimes fail because a portion of the metallization fuses or vaporizes (suffers burnout). Burnout susceptibility can vary significantly from component to component on a given wafer, regardless of design. This practice provides a procedure for establishing the limits of pulse current overstress within which the metallization of a given device should survive.

4.2 This practice can be used as a destructive test in a lot-sampling program to determine the boundaries of the safe operating region having desired survival probabilities and statistical confidence levels when appropriate sample quantities and statistical analyses are used.

NOTE 2—The practice may be extended to infer the survivability of untested metallization adjacent to the specimen metallization on a semiconductor die or wafer if care is taken that appropriate similarities exist in the design and fabrication variables.

5. Interferences

5.1 The level at which failure of metallization subjected to pulsed-current overstress occurs may be dependent on the temperature experienced by the semiconductor device. If significant differences in ambient temperature or heat sinking, or both, exist between one test situation and another, the results may not be representative.

NOTE 3—See Appendix X1 for a discussion of factors related to metallization heat sinking.

5.2 If probes are used to contact the metallization specimen, suitable precautions must be taken or the results may be misleading. The probes must not be allowed to come into contact with the area of metallization being characterized.

5.2.1 The use of Kelvin probe connections to make the resistance measurements is usually required to prevent contact resistance (at the current injection point) from interfering with the measurement.

5.2.2 Probe contacts with excessive contact resistance may cause damage at the point of contact. Such damage can interfere with the measurement.

5.3 If the test is used to infer the survivability of metallization on a wafer or die, the results could be misleading unless such factors as the following are identical: (*1*) metallization design geometry, (*2*) oxide step geometry, and (*3*) orientation of the metallization paths and oxide steps to the metallization source during deposition.

NOTE 4—The design and fabrication factors listed in 5.3 have been shown to be important for systems of aluminum metallization deposited on SiO_2/Si substrates. They are given as examples and are not intended to be all inclusive or necessarily to apply to all metallization systems to which this practice may be applied.

NOTE 5—Variations in oxide step geometry must be expected (see X1.4.2).

5.4 A step-stress pulsing schedule is not recommended. If such a schedule is used so that each specimen is subjected to successive pulses of increasing amplitude until failure occurs, the results could be misleading. It is possible that a pulse of the proper level can cause melting at a defect site without causing an open circuit; the molten metal may become redistributed so that the defect appears cured and will lead to failure on successive pulses.

6. Apparatus

6.1 *Current-Pulse Generator*—A source of rectangular current pulses capable of meeting the following requirements:

6.1.1 Risetime and falltime less than 10 % of the pulsewidth (full width at half maximum amplitude (FWHM)),

6.1.2 Impedance high enough with respect to the specimen metallization so that the pulse amplitude remains constant to within ±5 % between the end of the rise and beginning of the fall,

6.1.3 Jitter in the pulse amplitude and width less than ± 5 %,

6.1.4 Current amplitude and pulsewidth capability to provide pulses as agreed upon by the parties to the test, and

6.1.5 Single-pulse capability.

NOTE 6—Refer to Appendix X2 for information relating a rectangular pulse to an arbitrary pulse structure.

6.2 *Pulse-Monitoring Equipment*, as follows:

6.2.1 *Voltage-Monitoring Kelvin Probe*, for use in the circuit of Fig. 1, with risetime less than or equal to 5 % of the pulsewidth of the shortest pulse to be applied, and shunt capacitance sufficiently low so that the pulse shape is not distorted more than specified in 6.1:

6.2.2 *Voltage-Monitoring Resistor* (*R*, Fig. 1), with sufficiently low inductance, resistance, and shunt capacitance so that the generated pulse is not distorted more than specified in 6.1 and the value of the resistance is known within ±1 %.

6.2.3 *Current Probe*, for use in the circuit of Fig. 2, with risetime less than or equal to 5 % of the pulsewidth of the shortest pulse to be applied, with an ampere-second product sufficient to ensure nonsaturation for the amplitudes and durations of the pulses to be used and accurate within ±5 %.

6.3 *Pulse-Recording Equipment*, transient digitizer, oscilloscope with camera, storage oscilloscope, or other pulse recording means having a risetime less than 5 % of the width of the shortest test pulse used and capable of recording individual test pulses.

6.4 *Test Fixture*, providing means for the current pulse to be transmitted through the metallization specimen as well as through an equivalent resistance (see 9.5) without distortion of the pulse shape beyond that specified in 6.1. The test fixture must also provide a means for connecting the metallization specimen to the resistance-measuring equipment (see 6.5). The test fixture will contact the specimen through either standard component package leads or wafer probes. More than one test fixture may be used.

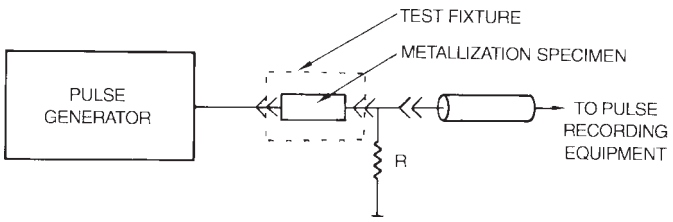

FIG. 1 Pulsing Circuit Using Resistor Voltage Drop to Monitor Current Through Specimen