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IEC 61523-1

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Delay and power calculation standards –

Part 1:
Integrated circuit delay and power calculation systems

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

DELAY AND POWER CALCULATION STANDARDS –

Part 1: Integrated circuit delay and power calculation systems

FOREWORD

1) The IEC (International Electrotechnical Commission) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of the IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, the IEC publishes International Standards. Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. The IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
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International Standard IEC 61523-1 has been prepared by IEC technical committee 93: Design automation.

This standard is based on IEEE Std P1481 (1999): *IEEE Standard for delay and power calculation systems*.

The text of this standard is based on the following documents:

FDIS	Report on voting
93/143/FDIS	93/144/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This standard does not follow the rules for the structure of international standards given in Part 3 of the ISO/IEC Directives.

IEC 61523 consists of the following parts, under the general title: *Delay and calculation standards:*

IEC 61523-1, Part 1: *Integrated circuit delay and power calculation systems*

IEC 61523-2, Part 2: *Prelayout delay calculation model specification of CMOS ASIC libraries* (to be published)

The committee has decided that the contents of this publication will remain unchanged until 2006. At this date, the publication will be

- reconfirmed;
- withdrawn;
- replaced by a revised edition, or
- amended.

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Introduction

The objective of the Delay and Power Calculation System (DPCS) is to make it possible for integrated circuit designers to *consistently* calculate chip delay and power across Electronic Design Automation (EDA) applications and for integrated circuit vendors to express delay and power information only *once* per technology while enabling sufficient EDA application accuracy.

This is accomplished by a coordinated set of standards which support a standard method to describe timing and power characteristics of integrated circuit design units (cells and higher level design elements); a standard method for EDA applications to calculate chip design instance specific delay, slew, and power for logic and interconnects; and standard file formats to exchange chip parasitic and cluster information.

A major integrated circuit design problem is to ensure the chip meets the designer's timing and power requirements. At this time in the EDA industry, there are numerous methodologies — many incompatible or inconsistent with each other — for representing timing and power information. The DPCS responds to the urgency to improve chip design methods.

The DPCS includes all aspects and uses of delay and power calculation (including synthesis, floorplanning, and simulation) during both pre-layout and post-layout phases of chip design. A fundamental requirement placed on the DPCS is that it work equally well with Verilog HDL and VHDL. In this draft of the standard, the scope of the DPCS is limited to integrated circuit designs.

The DPCS gains its leverage out of an effort by Silicon Integration Initiative (Si2) to standardize on contributed technology from IBM in the form of a Delay Calculation Language (DCL) and its companion procedural interface (PI), along with an effort by Open Verilog International (OVI) to standardize on file formats to exchange chip parasitic and cluster information in the form of a Physical Design Exchange Format (PDEF) and a Standard Parasitic Exchange Format (SPEF). SPEF is based on the Standard Parasitic Format (SPF) technology supplied by Cadence Design Systems. PDEF is based on technology provided by Synopsys.

Since each of these specifications is based on existing technology which has proven itself in industry, the time to introduce this standard into industry is greatly reduced over what would have been required for a newly created standard. The industry owes a great deal of gratitude to these companies for contributing these technologies.

The P1481 Working Group is composed of four subgroups: Architecture, Language, Parasitics and Clustering, and Power. The members of each of these groups are members of the P1481 Working Group. The P1481 Working Group has a vice-chair liaison with Japan to coordinate development and review of the specification there. The IEC TC93 WG 2 also participates in the review and development of this specification.

In addition to numerous individual contributors, both OVI, VHDL International (VI), and Si2 have played significant roles in the development of this standard and funding of the technical documentation.

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