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Standard Test Method for Characterizing Semiconductor Deep Levels by Transient Capacitance Techniques [1]

This standard is issued under the fixed designation F 978; the number immediately following the designation indicates the year of original adoption or, in the case of revision, the year of last revision. A number in parentheses indicates the year of last reapproval. A superscript epsilon (ε) indicates an editorial change since the last revision or reapproval.

1. Scope

1.1 This test method covers three procedures for determining the density, activation energy, and prefactor of the exponential expression for the emission rate of deep-level defect centers in semiconductor depletion regions by transient-capacitance techniques. Procedure A is the conventional, constant voltage, deep-level transient spectroscopy (DLTS) technique in which the temperature is slowly scanned and an exponential capacitance transient is assumed. Procedure B is the conventional DLTS (Procedure A) with corrections for nonexponential transients due to heavy trap doping and incomplete charging of the depletion region. Procedure C is a more precise referee technique that uses a series of isothermal transient measurements and corrects for the same sources of error as Procedure B.

1.2 *This standard does not purport to address all of the safety concerns, if any, associated with its use. It is the responsibility of the user of this standard to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use.*

2. Referenced Documents

2.1 *ASTM Standards:*

E 177 Practice for Use of the Terms Precision and Bias in ASTM Test Methods [2]

E 178 Practice for Dealing with Outlying Observations [2]

F 419 Test Method for Determining Carrier Density in Silicon Epitaxial Layers by Capacitance Voltage Measurements on Fabricated Junction or Schottky Diodes [3]

2.2 *Other Standard:*

MIL-STD-105 Sampling Procedures and Tables for Inspection by Attributes [4]

3. Summary of Test Method

3.1 In this method procedures are given for determining the density, activation energy, and the prefactor of the exponential expression for the emission rate of deep-level defect centers. In Procedure A (see Fig. 1), the temperature of the diode is slowly scanned while the bias voltage is repetitively changed. The high-frequency capacitance transient due to trap emission is sampled at two successively delayed gate times. The average difference between these sampled values constitutes the signal that has a maximum or peak at a temperature that is a function of the gate times. The time constant associated with the peak response is fixed by the rate window of the boxcar averager used to sample the transient or by computer simulation of such an instrument. For nonexponential transients, Procedure B adds a correction to the calculation of the time constant at the temperature of the response peak. In Procedure C, the temperature is held constant at each of a series of temperatures and the observed capacitance transient is analyzed for its corrected time constant. An Arrhenius-type semilogarithmic plot of normalized emission rate versus reciprocal temperature is made in each procedure, and the activation energy and prefactor are calculated from the slope and intercept, respectively. The density of the defects is determined from the magnitude of the capacitance changes.

3.2 The use of a boxcar averager is assumed in the discussion of Procedures A and B. However, a lock-in amplifier may also be used for these procedures, provided that factors which may degrade the results are taken into account. Constant-capacitance versions of these procedures are not discussed but are, of course, suitable for the purposes considered here. The nonexponential corrections covered in this test method are in general not needed for constant-capacitance measurements as the method itself eliminates most of the nonexponentiality.

4. Significance and Use

4.1 Deep-level defect measurement techniques such as isothermal transient capacitance (ITCAP) **(1, 2)** [5] and DLTS **(3)** utilize the ability of electrically active defects to trap free carriers and to re-emit them by thermal emission. Theoretically, the emission rate e_n for electrons is given by the following equation:

$$e_n = \sigma_n v_t N_c \exp(-\Delta G/kT)$$

[1] This test method is under the jurisdiction of ASTM Committee F01 on Electronics and is the direct responsibility of Subcommittee F01.06 on Electrical and Optical Measurement.

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[2] *Annual Book of ASTM Standards*, Vol 14.02.

[3] *Annual Book of ASTM Standards*, Vol 10.05.

[4] Available from Standardization Documents Order Desk, Bldg. 4 Section D, 700 Robbins Ave., Philadelphia, PA 19111-5094, Attn: NPODS.

[5] The boldface numbers in parentheses refer to the list of references at the end of this test method.

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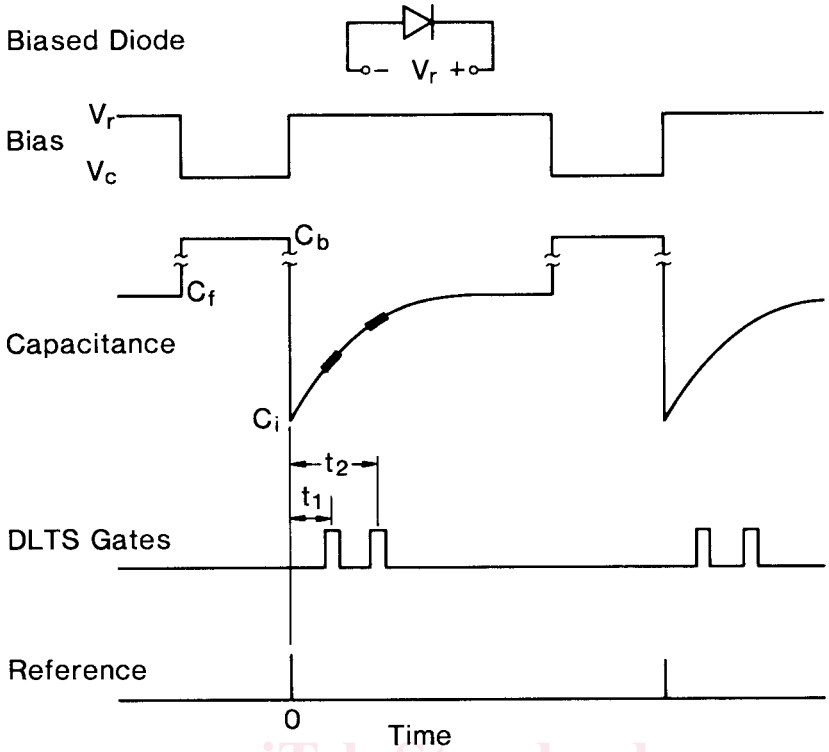

FIG. 1 Schematic of Biased n^+p Diode and Waveforms Associated with Repetitively Changing the Bias and Analyzing the Resulting Capacitance Transient

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where:

σ_n = capture cross section of the defect for an electron,
v_t = thermal velocity of the electron,
N_c = density-of-states in the conduction band,
ΔG = Gibbs free energy (a function of temperature) of the defect,
k = Boltzmann constant, and
T = absolute temperature.

4.2 A form commonly used for emission rate, $e_n = BT^2\exp(-\Delta E/kT)$, where B is assumed to be independent of temperature, is obtained by using $\Delta G = \Delta E - T\Delta S$, where ΔE is the activation energy (the enthalpy to be more exact which is the energy of the trap below the conduction band) and ΔS is the change in entropy **(4)**. For the equivalence of BT^2 to $\sigma_n v_t N_c \exp(\Delta S/k)$, one assumes σ_n and ΔS to have no dependence on temperature, a $T^{1/2}$ dependence for v_t, and a $T^{3/2}$ dependence for N_c. For ΔG to equal ΔE, $\Delta S = 0$ (that is, no change between the initial and final state degeneracy or lattice relaxation associated with the transition).

4.3 An analogous expression can be written for the hole emission rate. Analysis of the measured thermal emission rate in the depletion layer of a test device as a function of temperature leads to activation energies and effective capture cross sections of the defects present. The magnitude of the capacitance changes associated with the emission can be related to the densities of the defects present. The interest in measurement of deep levels in semiconductors stems from the following two related aspects:

4.3.1 Detection, identification, and control of unwanted native or process-induced impurities or defects; and

4.3.2 Characterization and control of impurities specifically introduced for lifetime or other parameter control.

5. Interferences

5.1 Temperature errors will significantly reduce the accuracy of the energy determination. Temperature inaccuracies that vary in magnitude with temperature are even more significant.

5.2 Nonexponentiality of the capacitance transient interferes with the characterization technique. Tests for nonexponentiality are given in 10.1. Causes of nonexponentiality are as follows:

5.2.1 The density of the deep-level defects is not small compared to the net shallow dopant density. Procedures B and C correct for this interference.

5.2.2 Trap charging does not take place throughout the depletion region at moderate (or higher) levels of trap density relative to net shallow dopant density. Procedures B and C correct for this interference.

5.2.3 The onset of free carriers at the edge of the depletion region is not sufficiently abrupt (that is, the approximation of complete depletion is not valid). Procedures B and C help correct for this.

5.2.4 The emission rate varies with electric field intensity (for example, Poole-Frankel effect).

5.2.5 The observed emission is the sum of emissions from two or more closely spaced and unresolved defect centers.

5.2.6 The response time of the capacitance meter, the recording system, or the test specimen (high resistance) is not negligible compared to the transient time constant.

5.3 Temperature dependencies of the capture cross section

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and the entropy change will introduce error in the proposed analysis.

6. Apparatus

6.1 *Capacitance Bridge or Meter*, using a high-frequency test signal and capable of measuring from 1 to 100 pF full scale with an accuracy as defined in Practice E 177 of ±0.5 % (1s %). Its response time should be much less than the smallest time constant to be measured. The instrument shall be capable of sustaining external dc bias of about ±50 V and have offset provisions for compensating or nulling out the external capacitance of the specimen holder, connecting cables, steady-state capacitance, etc. A provision for blocking out the large capacitance during the fill pulse is desirable. The capacitance measurement system used for determining the DLTS peaks in Procedures A and B does not need to be direct reading but must have an output that is sufficiently linear and a response time that is sufficiently fast to give undistorted peaks.

6.2 *Standard Capacitances*, of accuracy 0.25 % or better (1s %) at the measurement frequency. One capacitor shall be in the range from 1 to 10 pF and another in the range from 10 to 100 pF.

6.3 *Pulser*, with controllable repetition rate capable of changing from one bias voltage adjustable within the range of at least + 10 to − 10 V to another bias voltage in the same range. Switching time shall be much less than the smallest time constant to be measured and overshoot and undershoot shall be less than 1 % of pulse amplitude under operating conditions.

6.4 *Boxcar Averager*, or equivalent instrument (needed for Procedures A and B only) to process the capacitance transient. Desirable features are two separately controllable gate delay times with adjustable sampling time.

6.5 *Interval Timer*, (needed for Procedures A and B only) capable of measuring gate delay times of a few microseconds to several seconds with an accuracy of 0.1 % (1s %).

6.6 *Recorder System*, capable of digitally or continuously measuring and recording the following:

6.6.1 Capacitance as a function of time or temperature, or

6.6.2 The average difference in capacitance at two gate delay times as a function of temperature.

6.7 *Oscilloscope*, capable of observing the pulser output, the capacitance transient, and boxcar or other output to be recorded (not required but extremely helpful).

6.8 *Cryostat*, containing a specimen holder capable of maintaining a selectable temperature or of ramping the temperature up or down at a controlled rate. For silicon, the temperature range is usually between cryogenic and room temperature, and for gallium arsenide, the range is from cryogenic or room temperature to higher temperatures depending upon the energy levels of interest. In Procedure C, a radiation shield surrounding the specimen holder is necessary to attain temperature accuracy of 0.1 K at temperatures much below or much above room temperature.

6.9 *Thermometry System*, capable of determining the diode temperature with a precision of 0.1 K and an accuracy of 0.5 K for Procedures A and B and a precision of 0.02 K and an accuracy of 0.1 K for Procedure C.

7. Sampling

7.1 These procedures are nondestructive and are suitable for use on 100 % inspection. If a sampling basis is employed, the method of sampling shall be agreed upon by the parties to the test and shall be in accordance with acceptable statistical procedures (see MIL-STD-105).

8. Test Specimen

8.1 The procedures of this test method require that the deep levels to be characterized shall be in a depletable region of a semiconductor such as in a *p-n* junction diode or a Schottky diode. It is desira ble to use a peripheral guard ring suitably biased to isolate the depletion region of the device from surface states (see 10.2.1).

9. Calibration and Standardization

9.1 Measure the standard capacitances to determine that the capacitance bridge or meter is within specifications.

9.2 Verify time calibration by use of a calibrated time-mark generator or an interval timer for the recorder system. (For Procedure C only.)

9.3 Verify temperature calibration. Comparison with a calibrated platinum resistance thermometer under isothermal conditions is preferred. An alternative check is to use a well-characterized diode, lightly doped with platinum or another deep level (ΔE and B known), measure the emission rate $e_n = 1/\tau$, and calculate iteratively: $T = 11604.5\Delta\ E/(\ln\tau + 2\ \ln T + \ln B)$.

10. Procedure

10.1 *Tests for Nonexponentiality of the Capacitance Transients*—Use one or more of the following techniques:

10.1.1 *Thurber et al Technique* **(5)**—Choose a convenient value of rate window τ^{-1}, for example $(500\ \mu s)^{-1}$, and choose a sequence of values of t_2/t_1, for example, 2, 5, 10, 20, 50. Calculate for each value of t_2/t_1 as follows:

$$t_1 = \tau \cdot \ln (t_2/t_1)/(t_2/t_1 - 1)$$

then:

$$t_2 = t_1(t_2/t_1)$$

10.1.1.1 Perform 10.2.1 and 10.2.2 of Procedure A using the gate times t_1 and t_2 calculated here. Compare values of T_m from each run. If T_m is constant, the transient is exponential and the corrections of Procedure B are not needed; consequently follow Procedure A. If T_m changes with changes in the t_2/t_1 ratio, apply corrections by following Procedure B or use Procedure C.

10.1.2 *Manglesdorf Test* **(6)**—For a single capacitance transient, recorded at constant temperature, plot capacitance at time t against capacitance at a delayed time $t + \Delta t$ for several Δt values ranging from about 0.5 τ to a few τ . Calculate the slope m of the linear regression line fitted to the data points as follows:

$$m = (nZ_1 - X_1 \cdot Y_1)/(nX_2 - X_1{}^2)$$

where:

n = number of points,
X_1 = $\Sigma C\ (t)$,

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X_2 = $\Sigma[C(t)]^2$,
Y_1 = $\Sigma C(t + \Delta t)$, and
Z_1 = $\Sigma[C(t) \cdot C(t + \Delta t)]$.

10.1.2.1 Calculate $\tau = -\Delta t/\ln(m)$. If τ does not change as Δt is changed, the transient is exponential, and any of the procedures can be used. If τ changes as Δt is changed, Procedure B or C must be used.

10.1.3 Other analyses **(7)** suitable for computer automation are the fast Fourier transform method and the method of moments.

10.1.4 Following 10.4.5 through 10.4.9 of Procedure C, plot log C_n, where $C_n = (C - C_f)/(C_i - C_f)$, against time t. Linearity indicates that the capacitance transient is exponential, and any of the procedures can be used. Note that if C_i is difficult to measure, any initial value is all right. If the plot is not linear, Procedure B or C must be used.

10.2 *Procedure A (Normal DLTS)*:

10.2.1 For a diode with a guard ring, apply a peripheral-guard-ring bias equal to the flat-band voltage or select a voltage that minimizes the junction reverse leakage current. (Typically, this requires biasing into accumulation. Usually *n*-type silicon self-accumulates at 0 V.) Zero capacitance meter by substituting for specimen another diode whose only difference is a disconnected junction lead. For a probe system, zero capacitance meter with guard probe in contact but with junction probe raised to just break contact. (See Test Method F 419 for more details.) Make room temperature C^{-2} versus V plot over the range of voltages from zero to the largest reverse voltage planned. Calculate N_d(see 11.1).

10.2.2 Operate cryostat in the temperature ramping mode with a rate ≤0.1°C/s. Alternate bias between V_r and V_c repetitively (see Fig. 1). Plot the DLTS signal,$\langle C(t_1) - C(t_2)\rangle$, where the brackets denote an average over many repetitions, against temperature for a series (five or more) of gate times t_1 and t_2 such that $\tau = (t_2 - t_1)/\ln(t_2/t_1)$ spans a range of at least two decades and t_2/t_1 is between 2 and 10. (A larger t_2/t_1 ratio gives a larger signal.) Verify that the specimen temperature tracked the measured temperature by repeating the DLTS peaks for the highest and lowest temperatures. For this test decrease the temperature ramp rate by one-half or reverse the direction of the temperature ramp and look for a shift in peak temperature. If shifts are less than 0.2°C, continue with procedure; otherwise continue to vary ramp rate until a rate is found which, when doubled, introduces less than a 0.2°C systematic shift.

10.2.3 Measure temperature T_m at which signal peak is maximum. Record t_1, t_2, and T_m for each plot in the series. The gate times should be measured from the restoration of reverse bias to the middle of the sampling interval; that is, add one-half of the gate width to the observed t_1 and t_2 if the counter trigger is at the beginning of the gate. Calculate the following:

$$e^{-1} = \tau = \frac{t_2 - t_1}{\ln(t_2/t_1)}$$

10.2.4 Make Arrhenius plot (see 11.6.1).

10.2.5 Calculate and record activation energy of the defect level and its standard deviation, $\Delta E \pm s_{\Delta E}$(see 11.6.2 to 11.6.4).

10.2.6 Calculate and record prefactor of the exponential and its standard deviation, $B \pm s_B$(see 11.6.5).

10.2.7 To the extent possible, allow specimen to reach equilibrium at a temperature that will permit the recording of a capacitance transient that is affected as little as possible by the response time of the recording system.

10.2.8 Record transient and determine the following:

10.2.8.1 C_f, the capacitance at reverse voltage V_r;

10.2.8.2 C_b, the capacitance at charging voltage V_c; and

10.2.8.3 C_i, the capacitance when the reverse voltage is restored ($t = 0$).

10.2.9 Calculate and record N_t(see 11.7).

10.3 *Procedure B (DLTS With Corrections)*:

10.3.1 Perform 10.2.1 through 10.2.3 of Procedure A.

10.3.2 Apply charging bias voltage V_c. Measure and plot the capacitance at this voltage, C_b, versus temperature over the needed temperature range.

10.3.3 Repeat 10.3.2 with reverse bias voltage V_r(C_f versus T).

10.3.4 Determine the value of C_b and C_f at each temperature T_m or calculate C_b and C_f values using quadratic regression fits of the data (see 11.2).

10.3.5 Photograph the capacitance transient on an oscilloscope or record the output of a digital oscilloscope at each of several temperatures in the temperature range of interest. Measure the amplitude of the change in capacitance $\Delta C = C_f - C_i$ at each temperature. Calculate $C_i = C_f - \Delta C$ for each temperature. Interpolate to determine C_i at temperatures T_m or determine coefficients for a quadratic equation of C_i(see 11.2). Use the coefficients to calculate C_i at each temperature T_m.

10.3.6 Calculate and record the corrected time constant τ for each value of T_m (see 11.4).

10.3.7 Make Arrhenius plot (see 11.6.1).

10.3.8 Calculate and record activation energy of the defect level and its standard deviation, $\Delta E \pm s_{\Delta E}$(see 11.6.2 to 11.6.4).

10.3.9 Calculate and record prefactor of the exponential and its standard deviation, $B \pm s_B$(see 11.6.5).

10.3.10 At a selected temperature, use the values of C_f, C_b, and C_i determined in 10.3.4 and 10.3.5 to calculate N_t (see 11.7).

10.4 *Procedure C (Isothermal Measurements)*:

10.4.1 Perform 10.2.1.

10.4.2 Cool device to the lowest initial temperature anticipated and record that temperature. (Estimated values of temperature can be calculated from the equation in 9.3 and assumed values of ΔE and B.) Recheck zero of capacitance meter if practical and adjust if necessary. Make C^{-2} versus V plot.

10.4.3 Choose V_r to be in a nearly linear range of the C^{-2} versus V plot. The value of V_c is not critical but somewhat more accuracy can be obtained by avoiding values near 0 V provided that $C_f - C_i$ is easily measurable.

10.4.4 Make trial measurement of capacitance transient and decide on initial temperature.

10.4.5 Allow cryostat and specimen to reach temperature equilibrium at the chosen temperature under reverse bias V_r.

10.4.6 Measure and record capacitance (C_f) for reverse bias

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