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Standard Guide for Design of Flat, Straight-Line Test Structures for Detecting Metallization Open-Circuit or Resistance-Increase Failure Due to Electromigration[1]

This standard is issued under the fixed designation F 1259; the number immediately following the designation indicates the year of original adoption or, in the case of revision, the year of last revision. A number in parentheses indicates the year of last reapproval. A superscript epsilon (ε) indicates an editorial change since the last revision or reapproval.

1. Scope

1.1 This guide covers recommended design features for test structures used in accelerated stress tests, as described in Test Method F 1260, to characterize the failure distribution of interconnect metallizations that fail due to electromigration.

1.2 The guide is restricted to structures with a straight test line on a flat surface that are used to detect failures due to an open-circuit or a percent-increase in resistance of the test line.

1.3 This guide is not intended for test structures used to detect random defects in a metallization line.

1.4 Metallizations tested and characterized are those that are used in microelectronic circuits and devices.

2. Referenced Documents

2.1 *ASTM Standards:*

F 1260 Test Method for Estimating Electromigration Median-Time-To-Failure and Sigma of Integrated Circuit Metallizations[2]

F 1261 Test Method for Determining the Average Width and Cross-Sectional Area of a Straight, Thin-Film Metal Line[2]

3. Terminology

3.1 *Descriptions of Terms:*

3.1.1 *test chip*—an area on a semiconductor wafer containing one or more test structures having a specified or implied purpose.

3.1.2 *test structure*—a passive metallization structure, with terminals to permit electrical access, that is fabricated on a semiconductor wafer by the normal procedures used to manufacture microelectronic integrated devices.

4. Significance and Use

4.1 This guide is intended for the design of test structures used in measuring the median-time-to-failure and sigma (see Test Method F 1260) of metallizations fabricated in ways that are of interest to the parties to the test.

4.2 This guide is intended to provide design features that facilitate accurate test-line resistance measurements used in estimating metallization temperature. The design features are also intended to promote temperature uniformity along the test line when significant joule heating is produced during the accelerated stress test.

5. Design Features

5.1 The test structure shall have at least four terminals: two to conduct current and two to measure the voltage. The basic features are illustrated in Fig. 1.

5.1.1. The metallization to be characterized by the test structure shall be in the form of a straight test line of width w appropriate for the capability of the process and for the intended use.

NOTE 1—The median-time-to-failure and sigma (see Test Method F 1260) may be functions of the test-line width. This functional dependence may be affected by the size of the metallization grains.

5.1.2 The length of the test line shall be 800 µm. Adjacent-running lines may be included in the design to simulate actual-circuit layouts.

NOTE 2—To avoid interference in estimating $t50$ (see Test Method F 1260), where $t50$ may be a function of the length of the test line, a standard length of 800 µm is specified.[3]

NOTE 3—All dimensions specified here and elsewhere are designed dimensions. It is expected that the actual dimensions will differ somewhat due to processing.

5.1.3 Each end of the test line is contacted to a wider line of width $W = 2w$ that extends a distance L to a contact pad or other wide path for conducting the current to and from the test line. The length L shall be longer than 80 µm.

5.1.4 Each end-contact line shall have a voltage-tap line for measuring voltage. The width of the tap line shall be equal to or less than w, but not less than the minimum design width of the process. The distance from the center of the tap contact to the test line, Lt, shall be less than or equal to 8 µm. The length of each tap line shall be greater than 80 µm.

NOTE 4—The design features on the wider end-contact lines are for the purpose of reducing temperature gradients in the test line.

5.2 Test lines of adjacent electromigration test structures on a single semiconductor chip shall be separated from each other by a distance greater than ten times the thickness of the underlying electrical insulator on the semiconductor substrate.

5.3 A special test structure (see Test Method F 1261) for

[1] This guide is under the jurisdiction of ASTM Committee F-1 on Electronics and is the direct responsibility of Subcommittee F01.11 on Quality and Hardness Assurance.

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[2] *Annual Book of ASTM Standards*, Vol 10.04.

[3] Schafft, H. A., Staton, T. C., Mandel, J., and Shott, J. D., "Reproducibility of Electromigration Measurements," *IEEE Transactions in Electron Devices*, Vol ED-34, 1987, pp. 673–681.