Designation: F 1260 – 89

# Standard Test Method for Estimating Electromigration Median Time-To-Failure and Sigma of Integrated Circuit Metallizations[1]

This standard is issued under the fixed designation F 1260; the number immediately following the designation indicates the year of original adoption or, in the case of revision, the year of last revision. A number in parentheses indicates the year of last reapproval. A superscript epsilon (ε) indicates an editorial change since the last revision or reapproval.

## 1. Scope

1.1 This test method is designed to characterize the failure distribution of interconnect metallizations such as are used in microelectronic circuits and devices that fail due to electromigration under specified d-c current-density and temperature stress. This test method is intended to be used only when the failure distribution can be described by a log-Normal distribution.

1.2 This test method is intended for use as a referee method between laboratories and for comparing metallization alloys and metallizations prepared in different ways. It is not intended for qualifying vendors or for determining the use-life of a metallization.

1.3 The test method is an accelerated stress test of four-terminal structures (see Guide F 1259) where the failure criterion is either an open circuit in the test line or a prescribed percent increase in the resistance of the test structure.

1.4 This test method allows the test structures of a test chip to be stressed while still part of the wafer (or a portion thereof) or while bonded to a package and electrically accessible via package terminals.

1.5 This test method is not designed to characterize the metallization for failure modes involving short circuits between adjacent metallization lines or between two levels of metallization.

1.6 This test method is not intended for the case where the stress test is terminated before all parts have failed.

1.7 *This standard may involve hazardous materials, operations, and equipment. This standard does not purport to address all of the safety problems associated with its use. It is the responsibility of the user of this standard to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use.*

## 2. Referenced Documents

F 1259 Guide for Design of Flat, Straight-Line Test Structures for Detecting Metallization Open-Circuit or Resistance-Increase Failure due to Electromigration[2]

F 1261 Test Method for Determining the Average Width and Cross-Sectional Area of a Straight, Thin-Film Metal Line[2]

## 3. Description of Terms Specific to This Standard

3.1 *metallization*—the thin-film metallic conductor used as electrical interconnects in a microelectronic integrated circuit.

3.2 *test chip*—an area on a wafer containing one or more test structures that are stressed according to the test method while either still part of the wafer or after having been separated and packaged.

3.3 *test line*—a straight metallization line of designed uniform width that is subjected to the current-density and temperature stresses prescribed in the test method.

3.4 *test structure*—a passive metallization structure, with terminals to permit electrical access, that is fabricated on a semiconductor wafer by the normal procedures used to manufacture microelectronic integrated devices.

## 4. Summary of Test Method

4.1 This test method is used to obtain sample estimates of the median-time-to-failure, $t_{50}$, and sigma that describe the failure distribution of metallization test lines subjected to current-density and temperature stress. This involves subjecting a sample of $N$ test structures to high current-density and high ambient temperature stress, calculating the stress temperature of the metallization during the test, (which takes account of joule heating) and measuring the time to failure of each structure. The time-to-fail of the test structures is empirically described by a log-Normal distribution. The sample estimate of $t_{50}$ is equal to the exponential of the mean of the logarithm of the time-to-fail values as follows:

$$t_{50s} = \exp \overline{\ln t_f} \tag{1}$$

The sample estimate of sigma, $s$, is equal to the standard deviation of the logarithm of the time-to-fail values, scaled to remove the bias:

$$s = \left[1 + \frac{1}{4(N-1)}\right] \cdot \sqrt{\frac{\sum_{i=1}^{N} (\ln t_{fi} - \overline{\ln t_f})^2}{N-1}} \tag{2}$$

The failure times are plotted on a logarithm scale versus a Normal probability scale of cumulative percent failed to verify that the points plotted fall along a straight line and thereby demonstrate that they belong to a well-behaved, log-Normal distribution.

4.2 Before this test method can be implemented, a number of parameters must be selected and agreed upon by the parties to the test. These are the ambient stress temperature; the current-density stress; the temperature, $T_n$, to which the failure-time data shall be normalized (6.10); the failure criterion (6.3, 6.4, and 10.9.2); the number, $N$, of test structures to be stressed; the design-width of the test lines (3.3) to be stressed (6.11); and the activation energy, $E_A$ (6.10). Both $N$ and $s$ are used in 10.14 to determine the

[1] This test method is under the jurisdiction of ASTM Committee F-1 on Electronics and is the direct responsibility of Subcommittee F01.11 on Quality and Hardness Assurance.

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[2] *Annual Book of ASTM Standards*, Vol 10.04.

confidence limits for $t_{50}$ and sigma.

## 5. Significance and Use

5.1 Electromigration is a metallization failure mechanism that is of great concern especially for the reliability assessment of very large scale integrated (VLSI) microelectronic devices.

5.2 This accelerated stress test is used to obtain sample estimates of parameters that describe the failure distribution of the metallization at the stress conditions used in the test. These estimates are used in assessing metallization reliability and in making major decisions for the selection of metallization and processing technologies.

## 6. Interferences

6.1 Errors in estimating the mean current density and temperature stresses will lead to errors in the sample estimate of $t_{50}$ ($t_{50s}$) that can be calculated by the following empirical equation:

$$t_{50s} = A(1/J)^n \exp(E_a/kT) \quad (3)$$

where:

$A$ = constant,
$n$ = constant,
$J$ = mean current-density stress,
$E_a$ = activation energy (see 4.2),
$k$ = Boltzmann constant, and
$T$ = mean stress temperature of the test lines stressed.

For typical conditions, the induced percent error in $t_{50s}$ can be between two and three times the percent error in estimating $J$, and can be between 15 and 20 % if there is a 5°C error in estimating $T$ for temperatures between 150 and 200°C.[3]

6.2 Structure-to-structure deviations from the stress means produce changes in the time-to-fail, $t_f$, of the individual test structures. These changes lead to increases in $s$ and in the confidence limits for $t_{50}$ and sigma.[3] Deviations should be kept small enough that they do not produce changes in $t_f$ by more than 20 %.[3] This is especially important when sigma <0.4. The effect of stress deviations on $t_f$ is calculated from Eq. (3) by substituting $t_f$ for $t_{50s}$.

6.3 The effect of thermal interactions must be considered in estimating the mean stress temperature of the structures under test when more than one test structure on a test chip is stressed at a time and when joule heating is significant. These interactions are accounted for in 10.11. When the failure mode is a prescribed increase in resistance, separate corrections may be necessary if the currents to these structures have not been reduced and increases in the resistances of the failed structures during the remainder of the test produce significant increases in the power dissipation on the test chip. See 10.9.4 to avoid the need for these corrections.

6.4 The selection of a percent change in resistance as the failure criterion (4.2, 10.9.2) is required for a multilayered metallization that has a refractory metal layer. The value selected may affect significantly the measured activation energy, the value for $n$ in Eq. (3), and $t_{50s}$.[4] The use of a large percent increase in resistance (≳30 %) as the failure criterion may lead to undesirably large variability in test results[4] and to resistance oscillations due to open circuits in all but the refractory layer, especially when testing passivated metallizations.[5]

6.5 Some abnormalities in the test line and structure, other than those detectable from a visual inspection (7.2), may be indicated by an abnormal value for $R(TS)_L$ (10.3).

6.6 The voltage limit imposed on the test structure (8.1.4) is intended to reduce the possibility of the healing of an open circuit at the moment of failure.

6.7 It is possible, especially for passivated structures, that a test line, having failed due to an open circuit, will resume conduction spontaneously later in the test or when the stress conditions are interrupted for a period. The current to these structures shall be reduced as soon as practicable after their recovery has been detected.

6.8 The metallization to be tested must be sufficiently stable so that when it is subjected to the stress temperature of the test (but not the stress current), no significant change will occur with time in the resistance of the individual test structures or in the failure characteristics ($t_{50}$ and sigma) of the metallization due to electromigration.

6.9 The test is applicable only for cases where $t_{50}$ is large enough so that the resistance of the test structure under power, $R(TS)_P$, (10.8.1 and 10.8.3) can be measured before a significant change due to electromigration occurs in the resistance or in the temperature coefficient of resistance, TCR, (10.5) of the test structures under test.

6.10 The selection of the normalization temperature $T_n$ (4.2) can affect the accuracy of the sample estimate of $t_{50}$ to the extent that $T_n$ is different from the mean of the metallization stress temperatures of the test structures under test (10.12) and the estimate of the activation energy (4.2 and 6.1) is inaccurate.

6.11 When comparing different metallizations of similar thicknesses by their sample estimates of $t_{50}$, the test structures involved in the tests shall have test lines that have the same designed width. Otherwise, the possible dependence of $t_{50}$ on line width will interfere with such comparisons.

## 7. Preparatory Measurements

7.1 *Metallization Thickness*—Obtain an estimate of the metallization thickness from measurements made at five locations distributed over each wafer that is to provide test structures for the test method. This may be done after the metal deposition step with an appropriate contactless method or later on the wafer with a profilometer, for example. In the latter case, account for any consumption of the underlying dielectric or of the exposed metallization that may have occurred after the metallization deposition. Caution is also advised if a profilometer is used on passivated metallization; the deposition rate of the dielectric on the

[3] Schafft, H. A., Lechner, J. A., Sabi, B., Mahaney, M., and Smith, R., "Statistics for Electromigration Testing," *Proceedings International Reliability Physics Symposium*, 1988, p. 192.

[4] Ondrusek, J. C., Nishimura, A., Hoang, H. H., Sugiura, T., Blumenthal, R., Kitagawa, H., and McPherson, J. W., "Effective Kinetic Variations with Stress Duration for Multilayered Metallizations," *Proceedings International Reliability Physics Symposium*, 1988, p. 179.

[5] Maiz, J. A., and Sabi, B., "Electromigration Testing of Ti/Al-Si Metallization for Integrated Circuits," *Proceedings International Reliability Physics Symposium*, 1987, p. 145.

metallization may be different from the rate on other materials.

7.2 *Microscopic Inspection*—Perform a microscopic inspection of the test structures to be stressed. Reject structures intended for the test which have test lines that are discontinuous or have other abnormal physical features that can be observed. If structures are packaged, ensure that any package wire bonds electrically connecting the chip bonding pads to the package terminals do not touch other wire bonds or other parts of the test chip or package.

7.3 *Metallization Linewidth*—Obtain an estimate of the width of the test line.

7.3.1 The metallization linewidth shall be measured electrically using a special test structure (see Test Method F 1261). The test line of this structure shall be parallel to the test line of the structure to be tested as well as have the same designed line width and shall have the same local design features that can affect the width of the processed line.

7.3.2 If the stress test is to be performed on packaged test chips, the estimate of the line width shall be obtained from measurements of the special test structure that is included on the bonded chip and electrically accessible via the package terminals.

7.3.3 If the stress test is to be conducted on the wafer, the line width estimate shall be obtained from measurements of the special test structure that is located a distance from the electromigration test structures to be tested that is less than twice the diagonal dimension of the test chip or less than 5 mm, whichever is less.

7.4 *Metallization Cross-Sectional Area*—Calculate an average value for the cross-sectional area of the test lines to be stressed on a test chip by taking the product of the metallization thickness obtained from 7.1 and the line width from 7.3.

## 8. Test Circuit

8.1 The test circuit used shall have the following capabilities:

8.1.1 The current through each test structure shall be individually adjustable to the current necessary to attain the desired current density stress and be maintained constant during the stress test to within ±1 % of that current or 25 μA, whichever is greater (see 6.1 and 6.2).

8.1.2 The display resolution of the voltage if used to determine the current through a test structure shall be equivalent to 0.1 % of the intended stress current or 10 μV, whichever is greater (see 6.1.).

8.1.3 The display resolution of the voltage between the voltage taps of each test structure shall be equal to at least 0.1 % of the display voltage before and during the stress test when used to make resistance measurements (6.1). When used to monitor for open circuit failure, the display resolution of the voltage shall be at least 5 % of the display voltage.

8.1.4 The maximum voltage applied across the test structure during the stress test, and including the time of failure, shall be less than 15 V (see 6.6).

## 9. High-Temperature Stress Environment

9.1 *For a Packaged Test Chip*—A sensor with a display resolution of at least 0.5°C shall be used to measure the temperature of a heat sink in intimate thermal contact with the package. The point of measurement shall be within a distance $l$ from the perpendicular axis of the bonded chip, where $l$ is the length of one side of the chip.

9.2 *For Test Samples on a Wafer or Some Portion Thereof*—A sensor with a display resolution of at least 0.5°C shall be used to indicate the temperature of the heated surface used to produce the high temperature stress. This heated surface shall be in intimate thermal contact with the underside of the substrate. The difference between the temperature of the wafer top surface near where the structures to be tested are located and the temperature indicated by the sensor used to measure the heated surface shall be known within ±2°C (see 6.1).

9.3 The oven for the packaged devices or the heated surface for the wafer shall be able to maintain the high temperature environmental stress constant to within ±2°C for temperatures up to 200°C and within ±3°C for higher temperatures (see 6.1).

## 10. Procedure

10.1 Install test parts.

10.1.1 If packaged test samples are to be used, install packages in oven sockets fitted with heat sinks having a means for measuring the temperature near where the test chip is located in the package (9.1 and 9.3). Use a heat-conducting compound at the interface between package and heat sink to promote good heat transfer at the interface.

NOTE 1—It is suggested that the temperature of the heat sink be measured by a thermocouple inserted into a hole that has been drilled from one end of the heat sink to a point near where the test chip would be located.

10.1.2 If the test structures to be tested are on a wafer or a part thereof, employ a pressure-differential method to hold the substrate to the surface that is to be heated to the high temperature stress of the test (9.2 and 9.3).

10.2 Determine the thermal response time of the test system in the manner described in Annex 1 if packaged parts are to be used and if joule heating will be such that the mean value for $T(TS)_P - T(TS)_0$ will be greater than 2°C (see 10.7.1 and 10.8.4).

NOTE 2—The procedure in 10.2 can be performed earlier with an equivalent physical configuration and with equivalent packaged parts.

10.3 Measure the resistance, $R(TS)_L$, of each test structure at room temperature.

10.3.1 Ensure that the test structures are in thermal equilibrium with the local environment containing the sensors used to monitor the temperature.

10.3.2 Determine the temperature of the test structures, $T(TS)_L$.

10.3.2.1 If packaged samples are to be tested, measure the temperature of each package heat sink to determine the temperature of the structures in each package.

10.3.2.2 If the structures to be tested are on a wafer, determine the temperature of the top surface of the hot stage near where the structures are located.

10.3.3 Measure the resistance $R(TS)_L$ of each test structure at temperature $T(TS)_L$ using a current that is sufficiently small to produce negligible joule heating. To determine if joule heating is negligible, halve the current and remeasure the resistance. If no significant change in resistance is noted