

Designation: F 1263 – 99

Standard Guide for Analysis of Overtest Data in Radiation Testing of Electronic Parts ¹

This standard is issued under the fixed designation F 1263; the number immediately following the designation indicates the year of original adoption or, in the case of revision, the year of last revision. A number in parentheses indicates the year of last reapproval. A superscript epsilon (ϵ) indicates an editorial change since the last revision or reapproval.

1. Scope

1.1 This guide covers the use of overtesting in order to reduce the required number of parts that must be tested to meet a given quality acceptance standard. Overtesting is testing a sample number of parts at a stress higher than their specification stress in order to reduce the amount of necessary data taking. This guide discusses when and how overtesting may be applied to forming probabilistic estimates for the survival of electronic piece parts subjected to radiation stress. Some knowledge of the probability distribution governing the stressto-failure of the parts is necessary though exact knowledge may be replaced by over-conservative estimates of this distribution.

2. Referenced Documents

2.1 *Military Standards:*

- MIL-PRF 19500 Semiconductor Devices, General Specifications for²
- MIL-PRF 38535 Integrated Circuits (Microcircuit Manufacturing)²

3. Terminology

3.1 Description of Term: ai/catalog/standards/sist/1d18cc/

3.1.1 *confidence*—the probability, *C*, that at least a fraction, *P*, of the electronic parts from a test lot will survive in actual service; since radiation testing of electronic parts is generally destructive, this probability must be calculated from tests on selected specimens from the lot.

3.1.2 *rejection confidence*—the probability, R, that a lot will be rejected based on destructive tests of selected specimens if more than a specified fraction P of the parts in the lot will fail in actual service.

3.1.3 *Discussion of Preceding Terms*—Strictly speaking, most lot acceptance tests (be they testing by attributes or variables) do not guarantee survivability, but rather that inferior lots, where the survival probability of the parts is less than

probability, P, will be rejected with confidence, C. In order to infer a true confidence, it would require a Bayes Theorem calculation. In many cases, the distinction between confidence and rejection confidence is of little practical importance. However, in other cases (typically when a large number of lots are rejected) the distinction between these two kinds of confidence can be significant. The formulas given in this guide apply whether one is dealing with confidence or rejection confidence.

4. Summary of Guide

4.1 This guide is intended to primarily apply to sampling by attribute plans typified by Lot Tolerance Percent Defective (LTPD) tables given in MIL-PRF 38535 and MIL-PRF 19500, and contains the following:

4.1.1 An equation for estimating the effectiveness of overtesting in terms of increased probability of survival,

4.1.2 An equation for the required amount of overtesting given a necessary survival probability, and

4.1.3 Cautions and limitations on the method.

TM F15. Significance and Use

5.1 Overtesting should be done when (a) testing by variables is impractical because of time and cost considerations or because the probability distribution of stress to failure cannot be estimated with sufficient accuracy, and (b) an unrealistically large number of parts would have to be tested at the specification stress for the necessary confidence and survival probability.

6. Interferences

6.1 *Probability Distributions*—In overtesting, a knowledge of the probability distribution governing stress to failure is required, though it need not be specified with the same accuracy necessary for testing by variables. For bipolar transistors exposed to neutron radiation, the failure mechanism is usually gain degradation and the stress to failure is known to follow a lognormal distribution.³ For bipolar transistors exposed to total dose the use of the lognormal distribution is also

Copyright © ASTM International, 100 Barr Harbor Drive, PO Box C700, West Conshohocken, PA 19428-2959, United States.

¹ This guide is under the jurisdiction of ASTM Committee F-1 on Electronicsand is the direct responsibility of Subcommittee F01.11 on Quality and Hardness Assurance.

Current edition approved Dec. 10, 1999. Published February 2000. Originally published as F 1263 – 89. Last previous edition F 1263 – 94.

² Available from Standardization Documents Order Desk, Bldg. 4 Section D, 700 Robbins Ave., Philadelphia, PA 19111-5094, Attn: NPODS.

³ Messenger, G. C., Steele, E. L., "Statistical Modeling of Semiconductor Devices for the TREE Environment," *Transactions on Nuclear Science* NS-15, 1968, p. 4691.