INTERNATIONAL STANDARD

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First edition
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Information technology – Synchronous split transfer type system bus (STbus) – Logical layer

Technologies de l'information – Bus de système de transfert de fente synchrone (STbus) – Couche logique

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FOREWORD

ISO (the International Organization for Standardization) and IEC (the International Electrotechnical Commission) form the specialized system for worldwide standardization. National bodies that are members of ISO or IEC participate in the development of International Standards through technical committees established by the respective organization to deal with particular fields of technical activity. ISO and IEC technical committees collaborate in fields of mutual interest. Other international organizations, governmental and non-governmental, in liaison with ISO and IEC, also take part in the work.

In the field of information technology, ISO and IEC have established a joint technical committee, ISO/IEC JTC 1. Draft International Standards adopted by the joint technical committee are circulated to national bodies for voting. Publication as an International Standard requires approval by at least 75 % of the national bodies casting a vote.

International Standard ISO/IEC 14576 was prepared by subcommittee 26: Microprocessor systems, of ISO/IEC joint technical committee 1: Information technology.

International Standards are drafted in accordance with the rules given in the ISO/IEC Directives, Part 3.

Annexes A, B and C are for information only.

INFORMATION TECHNOLOGY –

SYNCHRONOUS SPLIT TRANSFER TYPE SYSTEM BUS (STbus) –

LOGICAL LAYER

1. Overview

1.1 Scope

This International Standard specifies the logical specifications of STbus which is a high-performance and highly reliable system bus. STbus adopts a synchronous transfer method with a high-speed clock and a split transfer method enabling to minimize bus holding time during one bus operation and to use a bus efficiently.

The contents given in this specifications are as follows:

a) System bus interface signal provisions;

b) Bus operations and transfer protocol for each bus operation;

c) Copyback cache coherency control for maintaining consistency between a shared memory and a cache memory of each processor in a multiprocessor system;

d) Fault detection function using parity check and duplex configuration for control signals.

1.2 Applicability

This International Standard is Applicable to a high-performance system bus or an I/O bus in a multiprocessor system. Typical STbus applications are indicated in Figure 1:

a) A System bus and an I/O bus in a TCMP system;

b) A System bus in an LCMP system.

- TCMP: tightly coupled multiprocessor system
  (A system consisting of two or more processors sharing the same memory, with the entire system controlled by one OS.)
- LCMP: loosely coupled multiprocessor system
  (A system in which each processor is connected by a shared memory or other medium, with each processor operated by an individual OS.)

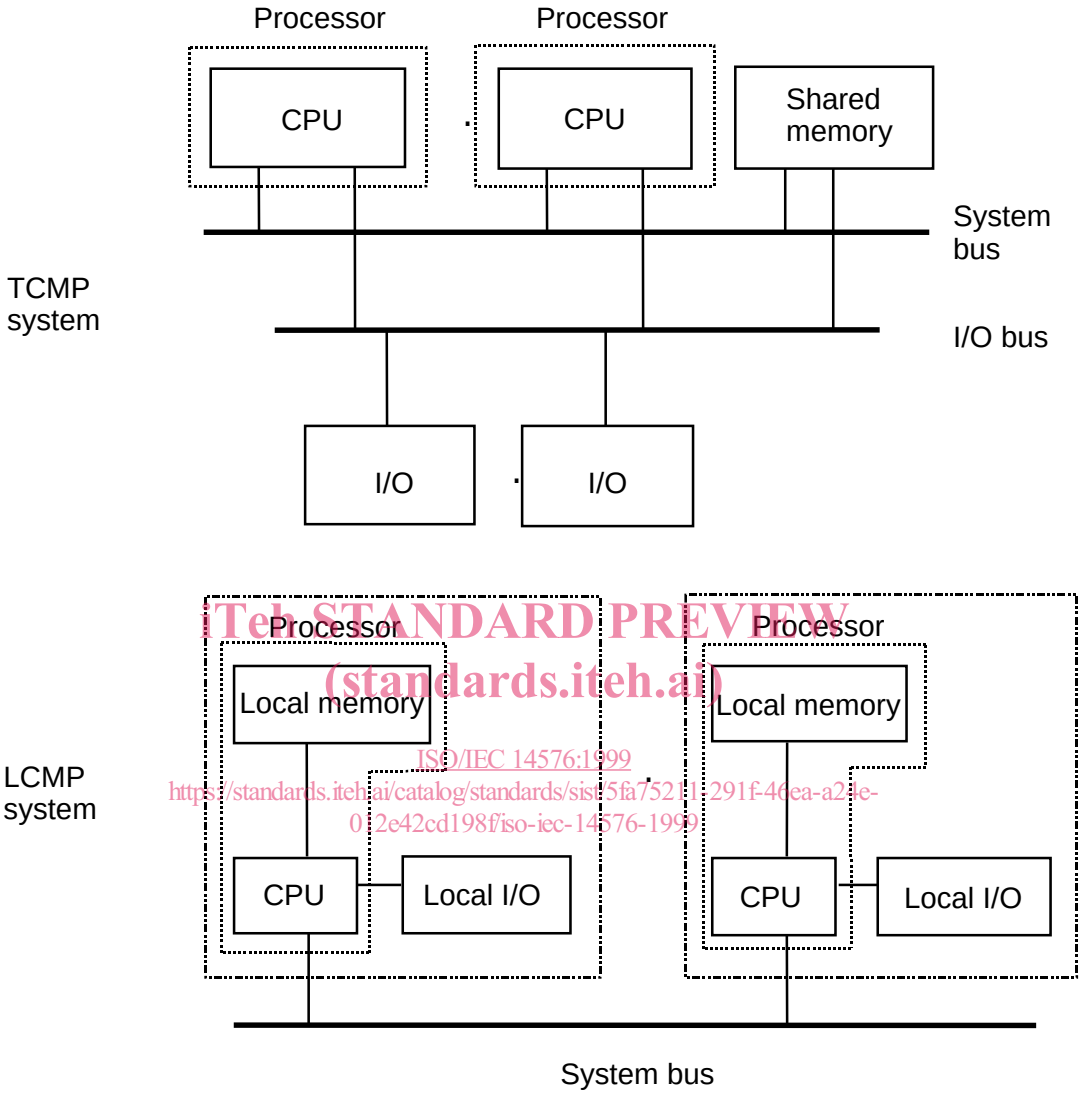


Figure 1 - STbus Applications

2. Definitions

2.1 Explanation of Terms

For the purposes of this International Standard, the following terms and definitions apply.

1) Answer transaction

An information transfer operation by which a function unit receiving a command returns answer information, to notify the unit issuing the command that the command has been completed (in some cases the requested data is appended) and to indicate status information.

2) Basic signal

Those bus interface signals that must be implemented in every STbus system, and thus for which compatibility is assured among different systems.

3) Block

The minimum unit registered in cache memory. In STbus this is limited to 32 bytes.

4) Bus handler (BH)

A concentrated bus control mechanism for sorting out competing bus requests from different function units, selecting one of the requests, and granting the bus right to that function unit.

5) Bus master

A function unit that has the bus right (a grant signal has been asserted) and is transferring information on the bus.

6) Bus slave

A function unit to which information is being transferred by the bus master.

7) Bus snoop

Monitoring of the bus for read operations from external memory and write operations to external memory.

8) Cache invalidation

A request to invalidate a block in cache memory. For example, when a write access is made to a Shared & Unmodified (SU) area, this is used to invalidate the same area in another cache.

9) CPU

A central processing element with functions for interpreting and executing instructions. In these specifications, cache memory is included with the CPU.

10) Copyback scheme

A cache updating method in which data written by the processor or instruction execution part is updated only in the cache, without being reflected directly in memory. The copyback

cache supported in STbus has the following three internal states: Invalid state (I), Shared & Unmodified state (SU), Exclusive & Modified state (EM).

11) DUT (Destination Unit)

A function unit performing an answer transaction.

12) Exclusive & Modified state (EM)

An internal state in a copyback cache, whereby the only place in the system an access area is registered is in cache memory, and the contents are not the same as shared memory. In this state, only the cache has been updated.

13) Function unit

A hardware unit connected to the bus and having a mechanism for bus interface control. Normally one function unit consists of one board.

14) I/O adapter

A function unit that controls I/O devices under control of a processor.

15) Invalid state (I)

A state in which an area accessed by the processor is not registered in cache memory.

16) Modified read command

A command issued to the system bus by a copyback cache memory when a write access by the processor results in a write miss.

17) Optional signal

Those bus interface signals that users are free to adopt or not in system implementation.

18) Order transaction

An information transfer operation for sending a command and requesting processing by another function unit.

19) Parity

When not otherwise noted in these specifications, parity is always odd. Here odd parity means that when a given signal (e.g., 8 bits) is augmented by a parity bit (e.g., 8 + 1 = 9 bits), then if the sum of 1-bits in the augmented set is an even number (including 0) an error is detected.

20) Processor

A function unit with the capability of executing instructions and controlling the various I/O adapters. Processor consists of CPU and memory in general.

21) Read hit/read miss

When an instruction or operand to be read by the processor is registered in cache memory, this is called a read hit. If not, it is a read miss.

In the case of a read miss, if the object of the read is cacheable, one block containing the object is newly registered in the cache.

22) Retry indication

The temporary suspension of access by external devices to a copyback cache area that has been updated without the change having been reflected in main memory.

23) Shared & Unmodified state (SU)

An internal state in a write-through or copyback cache, whereby an access area is registered in a cache and has the same contents as shared memory. Sharing by more than one cache is possible.

24) SUT (Source Unit)

A function unit performing an order transaction.

25) Write hit/write miss

If an area to be written by the processor is registered in cache memory, this is called a write hit. If not, it is a write miss.

In the case of a write-through cache, the write data is immediately reflected in shared memory.

If a copyback cache scheme is used, in the case of a write hit the write data is reflected in the cache only. If a write miss occurs, one block of the write area is read from shared memory and newly registered, then the write data is written over that area in the cache only.

26) Write-through scheme

A cache updating method in which data written by the processor or instruction execution part is reflected directly in memory. The internal states are: Invalid state (I), Shared & Unmodified state (SU).

2.2 Notation

The following symbols and other notation are used in these specifications.

- Function unit numbers are indicated by (#n), and control signals to each unit are written as [signal line name + (function unit number)], e.g., RQL*(#n), GR*(#n).
- When the values of control signals are indicated, the following notation is used.
  - When indicating the logical value of a signal line: 1 and 0 are used, with 1 meaning assert and 0 meaning negate.
  - When indicating the actual value on a signal line: "H" and "L" are used, with "H" meaning high and "L" meaning low signal potential.
- Hexadecimal notation in these specifications is indicated by H'## (e.g., H'FF, H'00).

3. Interface Specifications

3.1 Interface Signals

The STbus basic interface signals are listed in Table 1, as seen from one function unit.

In this table, RQL*, RQH*, GR*, and ET* are signals connected individually to each function unit.

Table 1 - Basic Interface Signals (function unit interfaces other than bus handler)

No.	Signal name	Count	Functional category	Connection type
1	RQL∗ (Request low)	1		
2	RQH∗ (Request high)	1	Arbitration control	Individually connected
3	GR∗ (Grant)	1		
4	ET∗ (End of bus transaction)	1		
5	BS∗ (Bus transaction start)	1		
6	BUR∗ (Burst)	1	Transfer control	
7	CSP∗ (Control signal parity)	1		
8	LCK∗ (Lock)	1		Bus connection
9	AD [00..63]∗ (Command/address/data)	64	Command/address/data	
10	ADP [0..7]∗ (AD parity)	8		
11	RTY∗ (Retry)	1	Cache coherency control	
12	RST∗ (Reset)	1	Reset signal	
13	CK (Clock)	1	Clock	See Note 2.
Total number of signals		83		

Note 1: A ∗ after a signal name indicates negative logic.

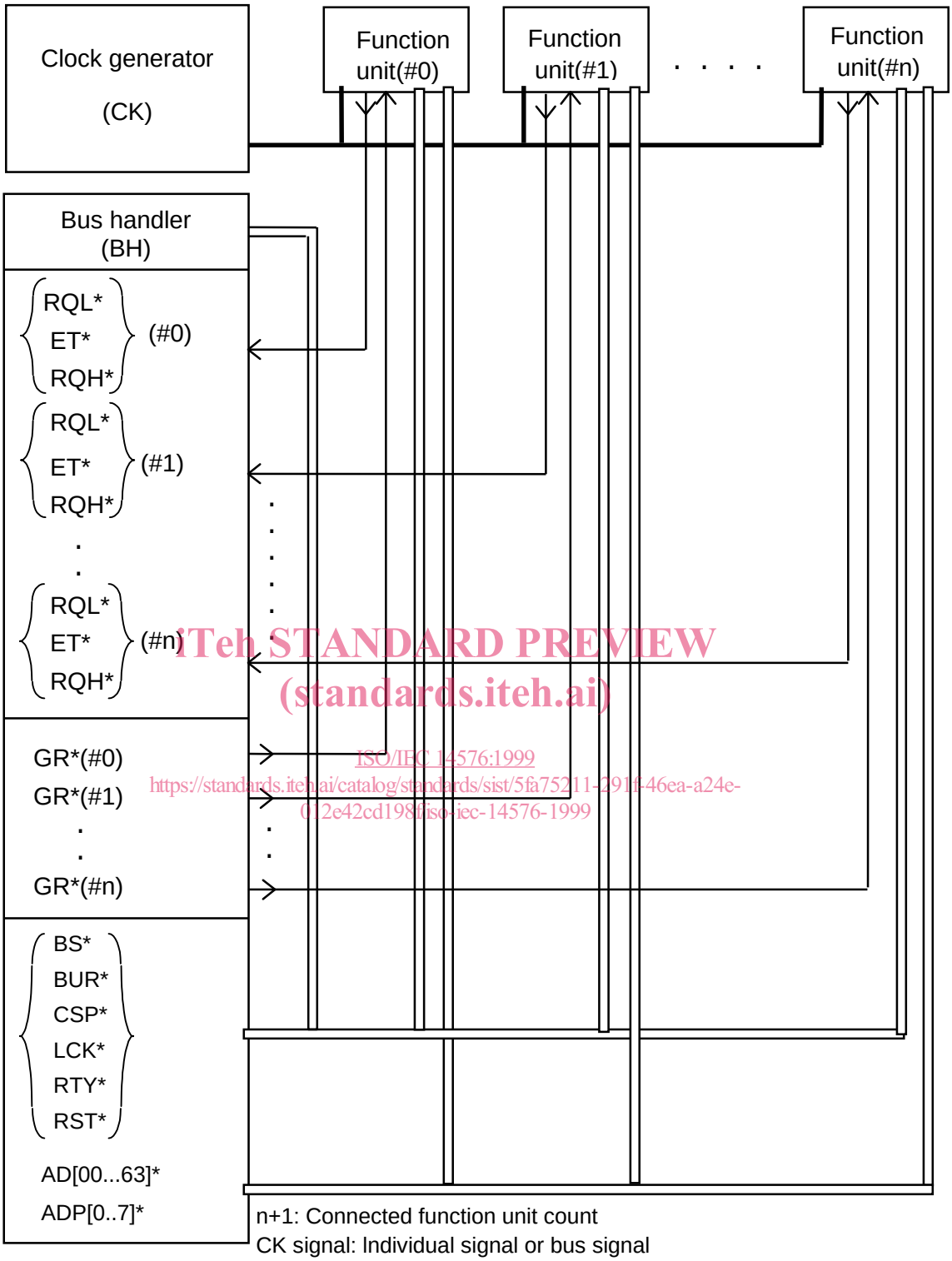
Note 2: For clock connection, a connection configuration must be adopted that can guarantee the skew specified in the physical specifications.

The optional interface signal lines as seen from one function unit are listed in Table 2. Since these signals are optional, the system implementor can choose whether or not to use them.

Table 2 - Optional Interface Signals (function unit interfaces other than bus handler)

No.	Signal name	Count	Functional category	Connection type
14	LCKS* (Lock spare)	1	Transfer control	
15	RTYS* (Retry spare)	1		Bus connection
16	STI* (Steal inhibit)	1	Cache coherency control	
17	STIS* (Steal inhibit spare)	1		

Connection structure



n+1: Connected function unit count
CK signal: Individual signal or bus signal
For clock connection, a connection configuration must be adopted that can guarantee the skew specified in the physical specifications.

Figure 2 - Connection interface between function units (basic pattern)