Designation: F 1388 – 92 (Reapproved 2000)

Standard Test Method for Generation Lifetime and Generation Velocity of Silicon Material by Capacitance-Time Measurements of Metal-Oxide-Silicon (MOS) Capacitors[1]

This standard is issued under the fixed designation F 1388; the number immediately following the designation indicates the year of original adoption or, in the case of revision, the year of last revision. A number in parentheses indicates the year of last reapproval. A superscript epsilon (ε) indicates an editorial change since the last revision or reapproval.

1. Scope

1.1 This test method covers the measurement of generation lifetime and generation velocity of silicon wafers.

1.2 The measurement requires the fabrication of a guard-ring MOS (Metal-Oxide-Silicon) capacitor. This test method is therefore destructive to the silicon wafer.

1.3 This test may also be applied to semiconductor materials other than silicon and to insulators other than silicon dioxide, but the details of capacitor fabrication and the analyses and interpretation of data in such cases are not given in this test method.

1.4 Both *p*- and *n*-type silicon in the doping range from 10^{13} to 10^{17} cm^{-3} can be evaluated by this test method. The approximate range of generation lifetime that can be measured is 1 µs to 10 ms.

1.5 The test method is applicable to both bulk and epitaxial silicon. If epitaxial silicon is used, the epitaxial layer must be of the same conductivity type as the substrate and should be at least twice as thick as the maximum depletion width in deep depletion to avoid errors caused by the proximity of the epitaxial interface (see 12.4).

1.6 It is necessary to complete the measurements described in Test Method F 1153 before performing the measurements described in this test method to determine the values of maximum capacitance, equilibrium minimum capacitance, and doping density.

1.7 A digital computer capable of controlling the instruments and recording data is required and significantly simplifies and improves the accuracy of the data acquisition and analysis process.

1.8 *This standard does not purport to address all of the safety problems, if any, associated with its use. It is the responsibility of the user of this standard to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use.* Specific hazard statements are given in 11.5 and 11.8.

2. Referenced Documents

2.1 *ASTM Standards:*

F 1153 Test Method for Characterization of Metal-Oxide-Silicon (MOS) Structures by Capacitance-Voltage Measurements[2]

F 1241 Terminology of Silicon Technology[2]

3. Terminology

3.1 *Definitions of Terms Specific to This Standard:*

3.1.1 *generation lifetime*—the average time to create an electron-hole pair in the space charge region of a reverse-biased MOS capacitor.

3.1.2 *generation velocity*—the component of the electron-hole pair carrier creation that is independent of the width of the depletion region. This component is a lumped term composed of electron-hole pair creation from the surface and the quasi-neutral bulk.

3.1.3 *guard ring*—a ring of metal surrounding an MOS capacitor that is spaced less than 10 µm from the periphery of the capacitor electrode and that can be biased independently from the capacitor electrode (see Fig. 1).

3.2 Other terms as defined in Terminology F 1241: Proper nomenclature for terms such as “equilibrium inversion capacitance”, “doping density” and other terms used in this test method and in Test Method F 1153 are currently under review and a common set is being developed. Until this set is defined, some differences between these test methods, Test Method F 1153, and Terminology F 1241 will exist.

4. Summary of Test Method

4.1 The small-signal high-frequency capacitance of an MOS capacitor is measured as a function of time, after the capacitor has been subjected to a voltage step from accumulation to inversion. The generation lifetime and generation velocity are determined from an analysis of the capacitance-time data.

4.2 The following assumptions are made in the analysis of the capacitance-time data to determine the generation lifetime and generation velocity:

4.2.1 The majority carrier density is zero within the depletion region and equal to the doping density outside; the

[1] This test method is under the jurisdiction of ASTM Committee F01 on Electronics and is the direct responsibility of Subcommittee F01.06 on Electrical and Optical Measurement.

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[2] *Annual Book of ASTM Standards*, Vol 10.05.

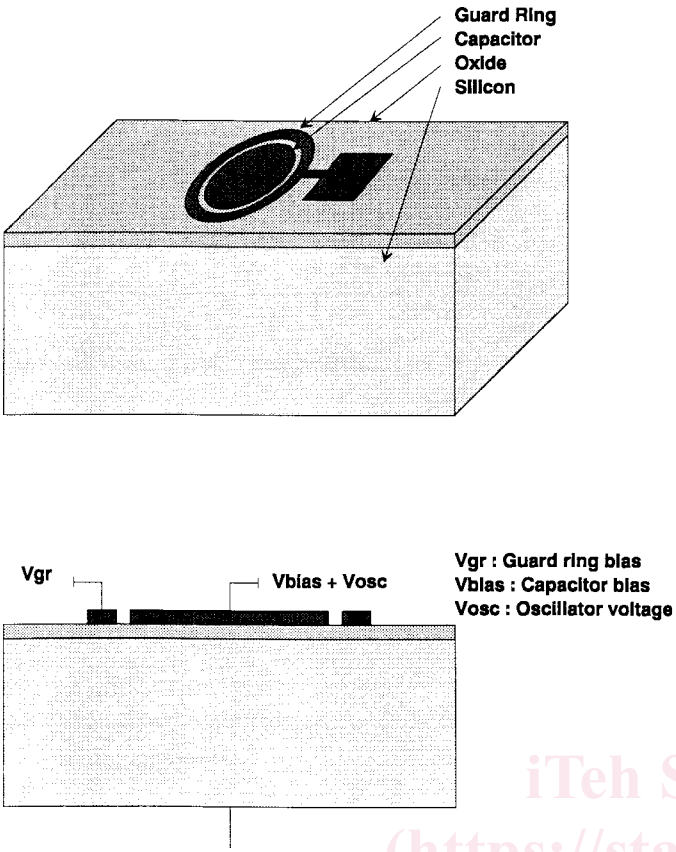

FIG. 1 Guard Ring Capacitor Diagrams

transition at the edge of the depletion region is a step function (depletion approximation).

4.2.2 The voltage drop across the inversion layer is zero.

4.2.3 The doping density of the silicon wafer (or epitaxial layer) is known and is constant throughout the wafer (or layer).

4.2.4 The relative dielectric constants of the silicon and of the silicon dioxide are known and constant throughout the materials.

5. Significance and Use

5.1 Generation lifetime and generation velocity are strongly influenced by electrically active deep-level impurities and physical imperfections in the silicon, and are thus an indication of the quality of the silicon wafer. Such electrically active deep-level impurities and physical imperfections can cause excessive *p-n* junction leakage, poor dynamic random access memory (RAM) refresh performance, and "dark current" degradation in computer-controlled display (CCD) memories, delay lines, filters, and imagers.

NOTE 1—The lifetime measured by this test method will be that of the processed material, not necessarily that of the virgin silicon. Extreme care needs to be taken to ensure that such aspects of MOS capacitor fabrication as pre-oxidation clean process gases, chemicals, and furnace quartzware do not introduce lifetime altering contaminants (see also 6.3.3).

5.2 This test method is suitable for monitoring the generation lifetime and generation velocity of silicon wafers in the following situations:

5.2.1 *Incoming and Outgoing Inspection of Silicon Wafers*—Due to the length of measurement time at room temperature and destructive nature of the test, such inspection should be restricted to a small number of wafers. In the absence of an interlaboratory evaluation of the precision of this test method, its use for materials acceptance is not recommended unless the parties to the test mutually agree on the method's repeatability and on the correlation they can obtain.

5.2.2 *Contamination Monitoring of Processing Equipment, Materials, or Procedures*—Such monitoring will require using silicon wafers of known generation lifetime and generation velocity, obtained from lots sampled by previous MOS capacitance-time characterization, to fabricate the MOS capacitors. The results can then be compared to the known material values to determine the effect of the processing. Due to variations in generation lifetime and generation velocity of typical groups of silicon wafers, a large number of measurements may be required to produce statistically significant results.

5.2.3 Research and development purposes for the evaluation of new materials, processes, and methods involved in the fabrication of semiconductor devices.

6. Interferences and Sources of Errors

6.1 *Instrumentation Errors*—Typical errors due to instrumentation include the following sources:

6.1.1 *Stray Capacitance, Inductance, Conductance, Resistance, and Phase Errors*—Errors are caused by excessive lengths of connecting cable between the capacitance meter and the measurement fixture. Carefully review and follow the capacitance meter or bridge manufacturer's recommendations regarding cable length and necessary correction factors.

6.1.2 *Improper Compensation of Stray Capacitance, Inductance, Conductance and Resistance Associated with the Measurement Fixture*—Such errors can cause the calculated value of the generation lifetime to increase, and in excessive cases, cause the calculated lifetime to be negative.

6.1.3 *Poor Bias Stability*—Any disturbance in bias during the measurement will result in errors. Some commercially available capacitance meters and bridges drop their internal bias supplies to zero volts during autoranging, causing errors in the capacitance-time characteristic.

6.2 *Measurement Fixture and Enclosure Errors*—Typical errors due to the measurement fixture and enclosure include the following sources:

6.2.1 *Poor Temperature Stability*—Such instability is typically due to stage motors, unbalanced thermal chucks, etc. Since the capacitance-time characteristic is strongly temperature-dependent, a known and stable capacitor temperature is essential. The temperature should vary by no more than 1°C during the measurement.

6.2.2 *Light Leaks*— High-quality MOS capacitors are extremely sensitive to low-level light (as their use in CCD imagers attests). *Every possible source of light must be eliminated*. This includes light from hinges, clear plastic vacuum lines, door edges, etc. Light leakage causes the calculated generation velocity to be increased due to electron-hole pair formation by the action of the light.

6.3 *MOS Capacitor Structure Related Errors*—Typical errors due to the MOS capacitor structure include the following sources:

6.3.1 *Lateral-Oxide-Surface-Charge-Spreading (LOSCS)*[3]—LOSCS is typically observed in thin silicon dioxide (1000 Å or less) MOS capacitors formed by shadow-masking of the metal gate. Adsorbed water molecules on the oxide surface allow dissociation of surface impurities into ionic forms, that respond to the applied gate bias, causing the oxide surrounding the metal dot to become charged. Such response is much slower than the applied oscillator voltage, thereby causing no additional contribution to the measured gate capacitance in accumulation or depletion. In inversion, however, the charged oxide can invert the silicon beyond the gate area. This extended inversion layer can then act as a source for minority carriers, causing the inversion layer under the gate to respond to the oscillator voltage. Such response causes the measured capacitance to increase as the LOSCS affects the oxide surface charge, causing gross errors in the measured capacitance-time characteristic. LOSCS results in artificially low values of generation lifetime and high values of generation velocity. Since the charge induced by LOSCS dissipates very slowly (on the order of days), LOSCS causes progressive deterioration of capacitance-time characteristics. LOSCS can be avoided by using a guard ring MOS capacitor (see Fig. 1). The guard ring is biased into accumulation at a voltage sufficient to prohibit LOSCS from affecting the inversion characteristics.

6.3.2 *Excessive Series Dissipation Factor*—Most commercial capacitance meters are sensitive to the dissipation factor of the capacitor being measured. The series dissipation factor, D_s, is defined by:

$$D_s = 2\pi f R_s C_s \qquad (1)$$

where:

f = measurement angular frequency, Hz,
R_s = series resistance, Ω, and
C_s = series capacitance, F.

When the dissipation factor exceeds some value specified by the capacitance meter manufacturer (usually 0.05 to 0.1), the capacitance measurement accuracy is significantly affected. High series dissipation factor can be caused by poor back side contact; high resistivity bulk silicon wafers; excessively large capacitors; excessively high measurement frequency.

6.3.3 *Processing Contamination*—This test method requires oxidation processing of the test wafer to form the MOS structure. In cases where the generation lifetime and generation velocity are being measured to determine the quality of outgoing or incoming silicon wafers, the utmost care must be taken to ensure that the fabrication of the MOS capacitor does not contaminate the test wafer with deep-level impurities, such as transition metals (see 5.1 and Note 1). Sources of contamination include any preoxidation cleans, processing gases or chemicals, and furnace quartzware.

7. Apparatus

7.1 *Facilities for Fabricating the MOS Capacitor*—As customarily used in the facility performing the test.

NOTE 2—Appendix X1 describes a process flow and structure that has been found to be suitable.

7.2 *Capacitance Bridge or Meter*—Capable of measurements from 1 to 1000 pF, or greater, full scale. The instrument shall have on each range an accuracy of 1.0 % of full scale or better and a reproducibility of 0.25 % of full scale or better. The small signal oscillator shall be adjustable to or fixed at a level of 0.010 to 0.050 VAC at a fixed or adjustable frequency in the range from 10 kHz to 1 MHz. The instrument shall supply or allow the application of d-c bias over the range of ± 100 VDC (see 7.4). The instrument shall be digital in nature and provide data to and be externally controllable by computer.

7.3 *Digital Voltmeter*—With ranges of 1 V full scale to 100 V full scale, a resolution of 0.1 % of full scale or better, an accuracy per range of 0.5 % of full scale or better, reproducibility of 0.25 % of full scale or better, input impedance of 100 MΩ or greater, and a common-mode rejection greater than 100 dB at 60 Hz. The instrument shall be digital in nature and provide data to and be externally controllable by computer.

7.4 *D-C Power Supply (Two)*—Capable of applying a step change in bias between any two voltages in the range of ± 100 V (open circuit) with a setting resolution of 10 mV or better and ripple of 0.5 % of the d-c output, or less. One of the supplies may be an integral part of the capacitance bridge or meter (see 7.1). The instruments shall be digital in nature and provide data to and be externally controllable by computer.

7.5 *Standard Capacitors (Two)*—Accurate to 0.25 % or better at the measurement frequency (see 7.2). One capacitor shall be in the range from 1 to 10 pF, inclusive and one shall be in the range from 10 to 100 pF, inclusive. The two capacitor values should differ by at least a factor of 10.

7.6 *Precision Voltage Source*—Capable of providing output voltages from 0 to ±100 V with an accuracy of 0.1 % of the output voltage or better.

7.7 *Thermometer (Digital or Analog) or Thermocouple*—With a range of 0 to 100°C and an accuracy of 0.5°C or better, to be attached to the metal chuck (see 7.8).

7.8 *Probe Fixture and Enclosure*—The fixture shall hold the test wafer and provide the following: probes for making contact to the gate and the guard ring, a metal chuck for back side contact, vacuum clamping of the test wafer to the chuck, and a means for attaching a thermometer or thermocouple to the chuck (see Fig. 2). The enclosure must be completely lighttight and constructed of metal for electrostatic shielding. The enclosure must provide a means for connecting coaxial cables from the exterior of the enclosure to the probe fixture within. The enclosure can be grounded either by contact to the outer shield of the coaxial cables connecting the capacitance meter or bridge to the probe fixture or by a separate connection from the enclosure to the chassis ground of the capacitance meter or bridge.

7.9 *Shielded Cables*— Of the correct characteristic impedance and length (as specified by the capacitance meter or bridge manufacturer) to connect the instruments together and avoid impedance mismatch errors.

7.10 *Ellipsometer*— The ellipsometer will be used to determine the oxide thickness of the MOS structure.

7.11 *Digital Computer*— Capable of controlling and recording data from the capacitance bridge or meter. A computer is

[3] Nicollian, E. H., Brews, J. R., *MOS (Metal Oxide Semiconductor) Physics and Technology*, Wiley-Interscience, 1982, pp. 148–156.