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INTERNATIONAL
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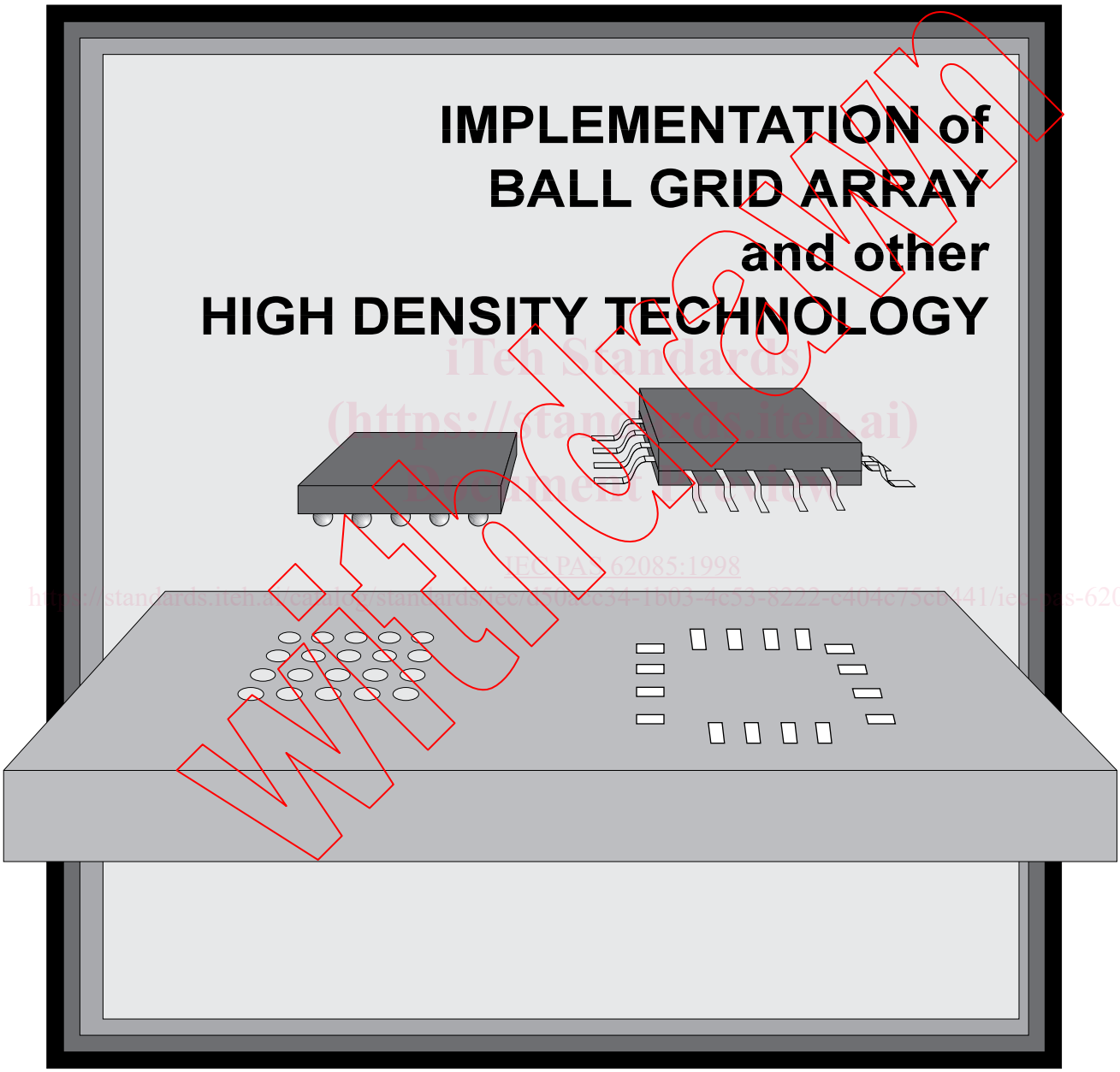

COORDINATED BY THE SURFACE MOUNT COUNCIL

IPC

SEMATECH

INTERNATIONAL ELECTROTECHNICAL COMMISSION

IMPLEMENTATION OF BALL GRID ARRAY AND OTHER HIGH DENSITY TECHNOLOGY

FOREWORD

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IEC-PAS 62085 was submitted by the IPC (The Institute for Interconnecting and Packaging Electronic Circuits) and has been processed by IEC technical committee 91: Surface mounting technology.

The text of this PAS is based on the following document:

This PAS was approved for publication by the P-members of the committee concerned as indicated in the following document:

Draft PAS	Report on voting
91/140/PAS	91/154/RVD

Following publication of this PAS, the technical committee or subcommittee concerned will investigate the possibility of transforming the PAS into an International Standard.

The following statement has been made by IPC (The Institute for Interconnecting and Packaging Electronic Circuits):

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The IEC and its members are authorized to exploit the following document:

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Material in this standard was voluntarily coordinated by the Surface Mount Council (SMC), and established by Technical Committees of IPC and EIA. Committee members of the two organizations contributed their time, knowledge and expertise to blend a cohesive report on the topic covered by this document. Proposals were sent to key individuals in each of the individual organizations for consensus. Meetings were held to resolve differences or conflicts prior to documenting the information in the final released version.

The material contained herein is advisory and its use or adaptation is entirely voluntary. IPC and EIA disclaim all liability of any kind as to the use, application, or adaptation of this material. Users are also wholly responsible for protecting themselves against all claims or liabilities for patent infringement.

Comments Welcome

The J-STD-013 is intended to serve as a roadmap for ball grid array and other high-density technology implementation.

In order to keep the document current, the Surface Mount Council welcomes comments from individuals reading the document, or implementing the suggested concepts.

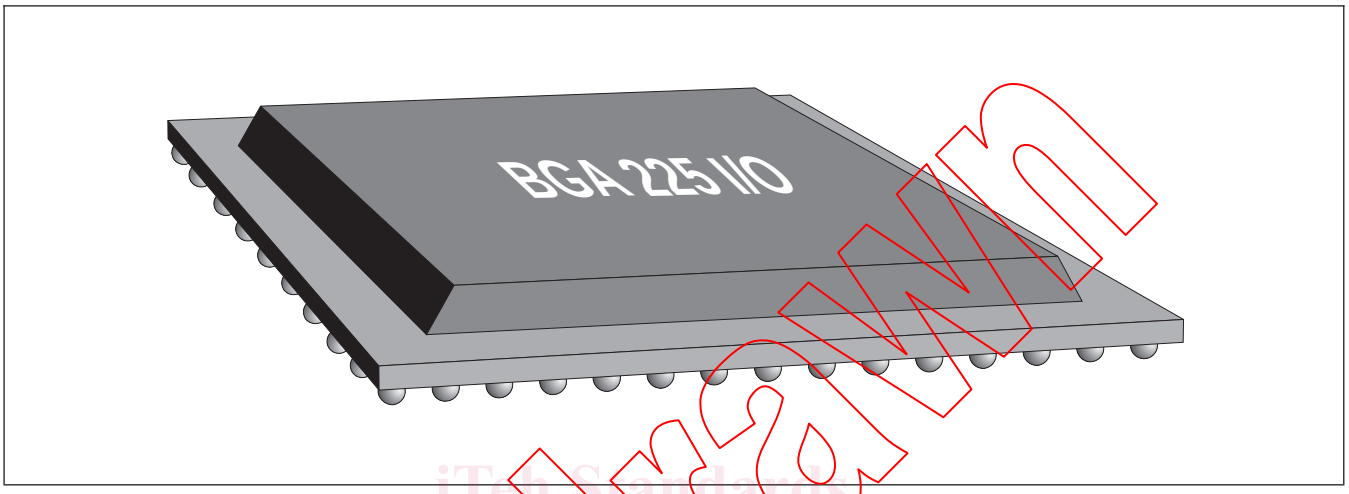
Comments may be sent to the EIA or IPC. All comments will be organized and sent to representatives of the Ad Hoc Committee responsible for the J-STD-013 for a yearly review and incorporation into the updating procedures.

Final Ballot Edition

The Surface Mount Council has authorized the special printing of this document in order to make the information available to industry experts for final ballot approval.

The official publication will be released for full industry circulation after the final editorial revision and completion of the balloting process by representatives of JEDEC. The results of those processes may initiate some changes. Once concensus has been reached, the official J-STD-013 will be printed and be supported by the three organizations, EIA, IPC, and JEDEC, and endorsed by Sematech and MCNC whose representatives participated and contributed to the development of this document.

J-STD-013
IMPLEMENTATION OF BALL GRID ARRAY AND OTHER HIGH-DENSITY TECHNOLOGY



About this Document

This document is intended to report on the work being done by a variety of organizations concerned with surface mounting of area array packages or other high pin count package configurations. The details were developed by companies who have implemented the processes described herein and have agreed to share their experiences. Readers are encouraged to communicate to the appropriate trade association any comments or observations regarding details published in this document, or provide additional ideas and details that would serve the industry.

Section 8 of this document represents a listing of standards that are being developed, being updated, or need to be created in order to provide for the orderly implementation of Ball Grid Array, or other High-Density Technology. Members of the industry are invited to participate in the ongoing standardization process.

For additional information regarding material published herein or inquiries regarding the status of standardization activities, we urge you to contact the organization listed below.

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Acknowledgement

Any standard involving a complex technology draws material from a vast number of sources. While the principle members of the Ad Hoc committee are shown below, it is not possible to include all of those who assisted in the evolution of this document. To each of them, the members of the IPC and EIA extend their gratitude.

Ball Grid Array Technology Ad Hoc Committee

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John Yantis, Texas Instruments

A special note of appreciation goes to the representatives of Intel who provided resources for a great deal of information regarding the subject of this publication, and to Motorola whose engineering personnel provided copies of their BGA mounting methodologies.

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Implementation of Ball Grid Array and Other High Density Technology

1 SCOPE

This document establishes the requirements and interactions necessary for Printed Board Assembly processes for interconnecting high performance/ high pin count I/C packages. Included is information on design principles, material selection, board fabrication, assembly technology, testing strategy, and reliability expectations based on end-use environments.

The focus of the document is on design through testing issues related to Ball Grid Array and other high performance packages including fine pitch, ultra fine pitch and thru-hole PGA.

1.1 Purpose

The purpose of this document is to provide confidence in the Design through Testing processes to ensure that the final assembly will meet the intended goals for product performance. Reliability is established through end use environments that consider the performance requirements of assemblies that are used in electronic products in such markets as consumer, computer, telecommunication, commercial aircraft, industrial & automotive passenger compartment, military ground & ship, space (both LEO and GEO), military avionics, and automotive underhood electronics and the customary use of those equipments.

1.2 Categorization

The details contained herein are organized according to the various issues and are correlated to the specific high pin count, high performance type I/C packages. These include:

- BGA Ball Grid Array
- CBGA Ceramic Ball Grid Array
- CCGA Ceramic Column Grid Array
- TBGA Tab Ball Grid Array
- MBGA Metal Ball Grid Array
- PPGA Plastic Pin Grid Array
- PGA Pin Grid Array (Standard and Staggered Pins)
- SGA Stud Grid Array (Surface Mount Version of PGA)
- LGA Land Grid Array
  - * Plastic
  - * Ceramic
- QFP Quad Flat Pack
- CQFP Ceramic Quad Flat Pack
- SSOP Shrink Small Outline Package
- TSOP Thin Small Outline Package
- TQFP Thin Quad Flat Pack
- FQFP Fine Pitch Quad Flat Pack
- LQFP Low Profile Quad Flat Pack
- SVP Surface Vertical Package (Post Stand/ Lead Stand)

Organization of the information is initially provided in accordance to the specific processes (i.e. Design-Fabrication-Assembly-Test). Component information is organized with emphasis on area array type packages. Although there is some discussion of the peripheral format, the major emphasis is on the decision process that forces the manufacturing direction into the area array type package. Table 1-1 indicates the packages of choice in various integration of semiconductor technology. Usually the trade-offs switch from peripheral packages to array type packages at 208 pins or below 0.5 mm pitch on the peripheral package.

Table 1–1 Choice of Packages

Semiconductor Integration	Number of Pins, Leads or Balls	Package Types
SSI	16-48	SOIC
MSI	48-156	QFP/PGA/BGA
LSI	156-256	BGA/QFP (0.5, 0.4, 0.3 mm pitch) and PGA
VLSI	256-500	BGA/PGA
ULSI	>500	BGA

1.3 Presentation

All dimensions and tolerances in this standard are expressed in metric units, with millimeters being the main form of dimensional expression. Inches may be shown in brackets as appropriate and are not always a direct conversion depending on the round-off concept or the required precision. Users are cautioned to employ a single dimensioning system and not intermix millimeters and inches. Reference information is shown in parentheses ( ).

1.4 Producibility Levels

The Surface Mount Council, in their ‘‘Status of the Technology, Industry Activities and Action Plan’’ identified several levels of complexity based on manufacturing and assembly processes for electronic assembly. A differentiation was developed that correlated the ease with which an assembly process could place, and attach all the parts and test the final product. Letters were assigned to reflect progressive increases in sophistication of tooling, materials or number of processing steps.

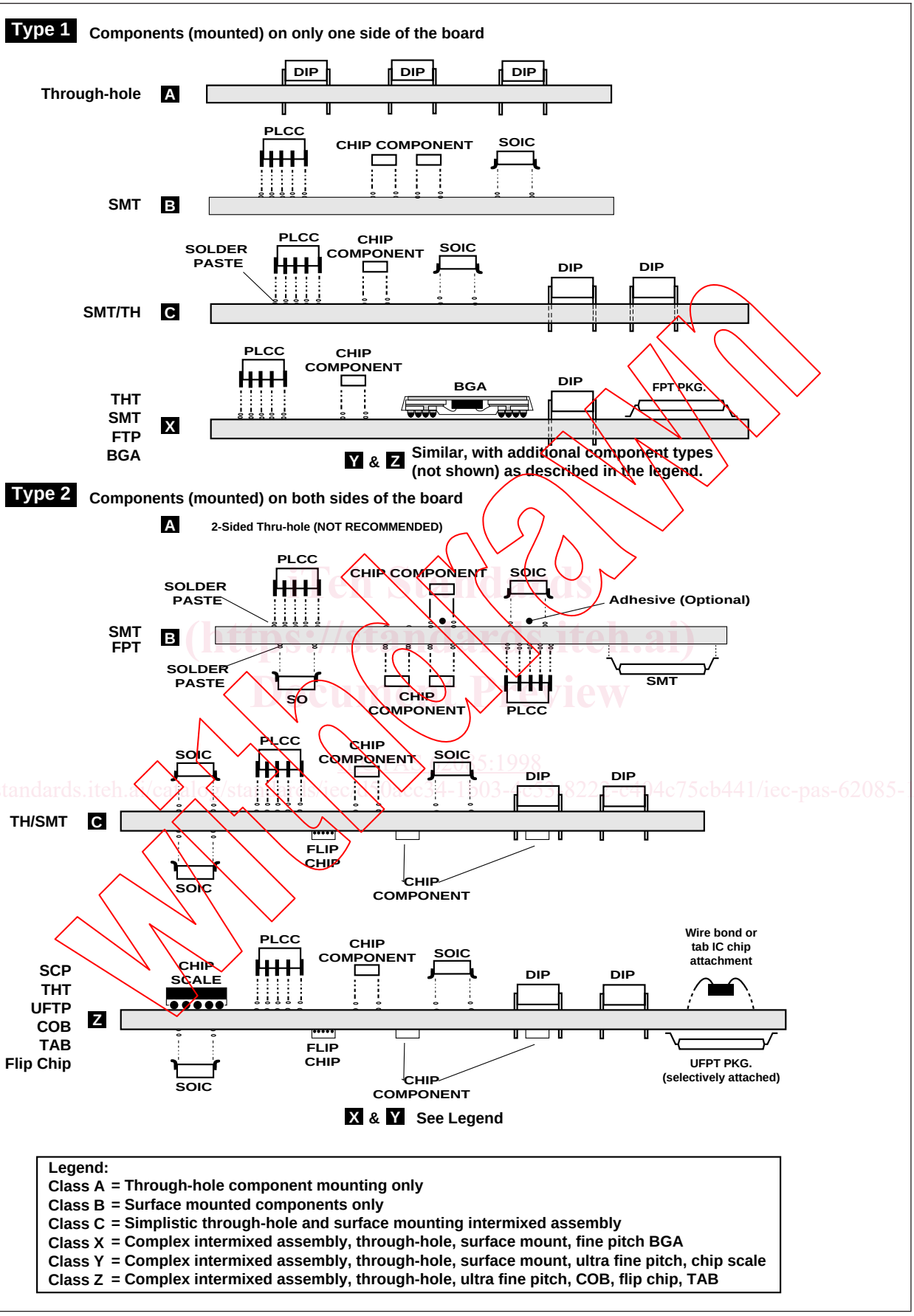

Figure 1−1 Electronic Assembly Types