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INTERNATIONAL STANDARD

NORME INTERNATIONALE

Test procedure of islanding prevention measures for utility-interconnected photovoltaic inverters

Procédure d'essai des mesures de prévention contre l'îlotage pour onduleurs photovoltaïques interconnectés au réseau public

IEC 62116:2008

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TEST PROCEDURE OF ISLANDING PREVENTION MEASURES FOR UTILITY-INTERCONNECTED PHOTOVOLTAIC INVERTERS

FOREWORD

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International Standard IEC 62116 has been prepared by IEC technical committee 82: Solar photovoltaic energy systems.

The text of this standard is based on the following documents:

FDIS	Report on voting
82/531/FDIS	82/542/RVD

Full information on the voting for approval can be found in the report on voting indicated in the above table.

The committee has decided that the contents of this publication will remain unchanged until the maintenance result date indicated on the IEC web site under "http://webstore.iec.ch" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

INTRODUCTION

Islanding is a condition in which a portion of an electric power grid, containing both load and generation, is isolated from the remainder of the electric power grid. This situation is one with which electric power providers (utilities) must regularly contend. When an island is created purposely by the controlling utility—to isolate large sections of the utility grid, for example—it is called an intentional island. Conversely, an unintentional island can be created when a segment of the utility grid containing only customer-owned generation and load is isolated from the utility control.

Normally, the customer-owned generation is required to sense the absence of utility-controlled generation and cease energizing the grid. However, when the generation and load within the segment are well balanced prior to the isolation event, the utility is providing little power to the grid segment, thus making it difficult to detect when the isolation occurs. Damage can occur to customer equipment if the generation in the island, no longer under utility control, operates outside of normal voltage and frequency conditions. Customer and utility equipment can be damaged if the main grid recloses into the island out of synchronization. Energized lines within the island present a shock hazard to unsuspecting utility lineworkers who think the lines are dead.

The PV industry has pioneered the development of islanding detection and prevention measures. To satisfy the concerns of electric power providers, commercially-available utility-interconnected PV inverters have implemented a variety of islanding detection and prevention (also called anti-islanding) techniques. The industry has also developed a test procedure to demonstrate the efficacy of these anti-islanding techniques; that procedure is the subject of this document.

This standard provides a consensus test procedure to evaluate the efficacy of islanding prevention measures used by the power conditioner of utility-interconnected PV systems. Note that while this document specifically addresses inverters for photovoltaic systems, with some modifications the setup and procedure may also be used to evaluate inverters used with other generation sources or to evaluate separate anti-islanding devices intended for use in conjunction with PV inverters or other generation sources acting as or supplementing the anti-islanding feature of those sources.

Inverters and other devices meeting the requirements of this document can be considered non-islanding, meaning that under reasonable conditions, the device will detect island conditions and cease to energize the public electric power grid.

TEST PROCEDURE OF ISLANDING PREVENTION MEASURES FOR UTILITY-INTERCONNECTED PHOTOVOLTAIC INVERTERS

1 Scope and object

The purpose of this International Standard is to provide a test procedure to evaluate the performance of islanding prevention measures used with utility-interconnected PV systems.

This standard describes a guideline for testing the performance of automatic islanding prevention measures installed in or with single or multi-phase utility interactive PV inverters connected to the utility grid. The test procedure and criteria described are minimum requirements that will allow repeatability. Additional requirements or more stringent criteria may be specified if demonstrable risk can be shown. Inverters and other devices meeting the requirements of this standard are considered non-islanding as defined in IEC 61727.

This standard may be applied to other types of utility-interconnected systems (e.g. inverter-based microturbine and fuel cells, induction and synchronous machines). However, technical review may be necessary for other than inverter-based PV systems.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 61727, *Photovoltaic (PV) systems – Characteristics of the utility interface*

IEC 61836, *Solar photovoltaic energy systems – Terms, definitions and symbols*

3 Terms and definitions

For the purposes of this document, the terms and definitions of IEC 61836 apply as well as the following.

3.1
PV array simulator
DC power source used to simulate PV array output

3.2
EUT (Equipment Under Test)
EUT indicates the inverter or anti-islanding device on which these tests are performed

3.3
MPPT (Maximum Power Point Tracking)
MPPT is a PV array control strategy used to maximize the output of the system under the prevailing conditions

3.4
non-islanding inverter
an inverter that will cease to energize a utility distribution system that is out of the nominal operation specifications for voltage and/or frequency (from IEC 61727 Ed. 2.0)

3.5
island

a state in which a portion of the electric utility grid, containing load and generation, continues to operate isolated from the rest of the grid. The generation and loads may be any combination of customer-owned and utility-owned.

3.6
intentional island

an island that is intentionally created, usually to restore or maintain power to a section of the utility grid affected by a fault. The generation and loads may be any combination of customer-owned and utility-owned, but there is an implicit or explicit agreement between the controlling utility and the operators of customer-owned generation for this situation.

3.7
quality factor, Q_f

a measure of the strength of resonance of the islanding test load.

NOTE In a parallel resonant circuit, such as a load on a power system

$$Q_f = R\sqrt{\frac{C}{L}}$$

where

Q_f is quality factor

R is effective load resistance

C is reactive load capacitance (including shunt capacitors)

L is reactive load inductance

With C and L tuned to the power system fundamental frequency, Q_f for the resonant circuit drawing real power, P, reactive powers Q_L, for inductive load and Q_C for capacitive load, Q_f can be determined by

$$Q_f = (1/P)\sqrt{|Q_L| \cdot |Q_C|}$$

where

P is real power, in W

Q_L is inductive load, in VAr_L

Q_C is capacitive load, in VAr_C

3.8
run-on time, t_R

the amount of time that an unintentional island condition exists. Run-on time is defined as the interval between the opening of the switch S1 (Figure 1) and the cessation of EUT output current.

3.9
stopping signal

a signal provided by the inverter indicating it has ceased energizing its utility grid-connected output terminals (see Annex C)

3.10
unintentional island

an islanding condition in which the generation within the island that is supposed to cease energizing the utility grid instead continues to energize the utility grid

4 Testing circuit

The testing circuit shown in Figure 1 shall be employed. Similar circuits shall be used for three-phase output.

Parameters to be measured are shown in Table 1 and Figure 1. Parameters to be recorded in the test report are discussed in Clause 7.

Table 1 – Parameters to be measured in real time

Parameter	Symbol	Units
EUT DC input [1,2]		
DC voltage	V_{DC}	V
DC current	I_{DC}	A
DC power	P_{DC}	W
Irradiance[3]	G	W/m²
EUT AC output		
AC voltage [2, 4, 5]	V_{EUT}	V
AC current [2, 4, 5]	I_{EUT}	A
Real power[2]	P_{EUT}	W
Reactive power[2]	Q_{EUT}	VAr
Voltage waveform [4, 5, 6, 7]		
Current waveform [4, 5, 6, 7]		
EUT (relay) output control signal [4]		
Run-on time	t_{R}	s
Stopping signal[8]	SS	--
Test load[2]		
Resistive load current	I_{R}	A
Inductive load current	I_{L}	A
Capacitive load current	I_{C}	A
AC (utility) power source[2]		
Utility real power[9]	P_{AC}	W
Utility reactive power[9]	Q_{AC}	VAr
Utility current[9]	I_{AC}	A

[1] If applicable.

[2] Record values measured before switch S1 is opened.

[3] Recorded when the test is carried out using a PV array. Pyranometer should be fast response silicon-type not thermopile-type.

[4] The response time of voltage and current transducer shall be suitable for the sampling rate used.

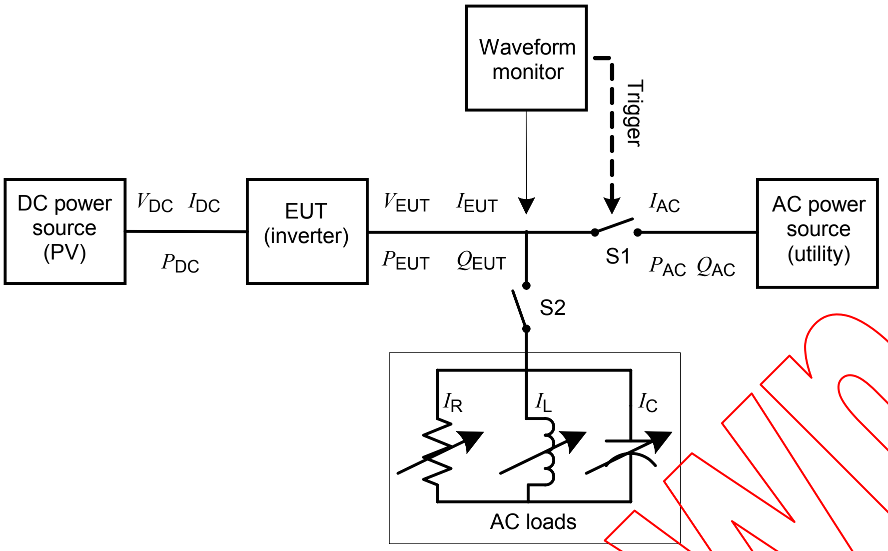
[5] The waveform, AC voltage and current, shall be measured on all phases.

[6] The waveform data shall be recorded from the beginning of the islanding test until the EUT ceases output. The measurement of time shall have an accuracy and resolution of better than 1 ms.

[7] When the waveform is recorded, the synchronizing signal of the S1 opening and stopping signal may be simultaneously recorded.

[8] If available from the EUT.

[9] Signal shall be filtered as necessary to provide fundamental (50 Hz or 60 Hz) frequency value. Fundamental values will ignore incidental harmonics, caused by utility voltage distortion, absorbed by the load and EUT filtering capacitors.



IEC 1567/08

Figure 1 – Test circuit for islanding detection function in a power conditioner (inverter)

5 Testing equipment

5.1 Measuring instruments

Waveform observation shall be measured by a device with memory function, for example, a storage or digital oscilloscope or high speed data acquisition system. The waveform measurement/capture device shall be able to record the waveform from the beginning of the islanding test until the EUT ceases to energize the island. For multi-phase EUT, all phases shall be monitored. A waveform monitor designed to detect and calculate the run-on time may be used.

For multi-phase EUT, the test and measurement equipment shall record each phase current and each phase-to-neutral or phase-to-phase voltage, as appropriate, to determine fundamental frequency real and reactive power flow over the duration of the test. A sampling rate of 10 kHz or higher is recommended. The minimum measurement accuracy shall be 1 % or less of rated EUT nominal output voltage and 1 % or less of rated EUT output current. Current, real power, and reactive power measurements through switch S1 used to determine the circuit balance conditions shall report the fundamental (50 Hz or 60 Hz) component.

5.2 DC power source

A PV array or PV array simulator (preferred) may be used. If the EUT can operate in utility-interconnected mode from a storage battery, a DC power source may be used in lieu of a battery as long as the DC power source is not the limiting device as far as the maximum EUT input current is concerned.

The DC power source shall provide voltage and current necessary to meet the testing requirements described in Clause 6.

5.2.1 PV array simulator

A unit intended to be energized directly from a photovoltaic source shall be energized from a supply that simulates the current-voltage characteristics and time response of a photovoltaic array. The tests shall be conducted at the input voltage defined in Table 2 below, and the current shall be limited to 1,5 times the rated photovoltaic input current, except when specified otherwise by the test requirements.

A PV array simulator is recommended, however, any type of power source may be used if it does not influence the test results.

Table 2 – Specification of array simulator (test conditions)

Items 1)	Conditions
Output power	Sufficient to provide maximum EUT output power and other levels specified by test conditions of Table 5.
Response speed2)	The response time of a simulator to a step in output voltage, due to a 5 % load change, should result in a settling of the output current to within 10 % of its final value in less than 1 ms.
Stability	Excluding the variations caused by the EUT MPPT, simulator output power should remain stable within 2 % of specified power level over the duration of the test: from the point where load balance is achieved until the island condition is cleared or the allowable run-on time is exceeded.
Fill factor 3)	0,25 to 0,8

1) For the purpose of this standard, it is assumed that there is no influence of cell technology on islanding detection.

2) Response speed is indicated to avoid influence caused by MPPT control system, ripple frequency on DC side of a EUT, or active methods of anti islanding.

3) Fill factor = $(V_{mp} \times I_{mp})/(V_{oc} \times I_{sc})$, where V_{mp} and I_{mp} are the maximum power point voltage and current, respectively, V_{oc} is the open circuit voltage, and I_{sc} is the short circuit current. It should be maintained at one value for all test conditions.

5.2.2 Current and voltage limited DC power supply with series resistance

A DC power source used as the EUT input source shall be capable of EUT maximum input power (so as to achieve EUT maximum output power) at minimum and maximum EUT input operating voltage.

The power source should provide adjustable current and voltage limit, set to provide the desired short circuit current and open circuit voltage when combined with the series and shunt resistance described below.

A series resistance (and, optionally, a shunt resistance) should be selected to provide a fill factor within the range shown in Table 2.

5.2.3 PV array

A PV array used as the EUT input source shall be capable of EUT maximum input power at minimum and maximum EUT input operating voltage. Testing is limited to times when the irradiance varies by no more than 2 % over the duration of the test as measured by a silicon-type pyranometer or reference device. It may be necessary to adjust the array configuration to achieve the input voltage and power levels prescribed in 6.1.

Table 3 – PV array test conditions

Items	Conditions
Output power	Sufficient to provide maximum EUT output power and other levels specified by test conditions of Table 5.
Climate condition	Irradiance, ambient temperature, etc.

To achieve a balanced load condition, the output of the PV array shall be stable. Thus, it is important to perform the test only during times of stable irradiance (e.g., clear sky, near solar noon).

5.3 AC power source

The utility grid or other AC power source may be used as long as it meets the conditions specified in Table 4.

Table 4 – AC power source requirements

Items	Conditions
Voltage	Nominal ±2,0 %
Voltage THD	< 2,5 %
Frequency	Nominal ±0,1 Hz
Phase angle distance 1)	120 ° ± 1,5 °

1) Three-phase case only

5.4 AC loads

On the AC side of the EUT, variable resistance, capacitance, and inductance shall be connected in parallel as loads between the EUT and the AC power source. Other sources of load, such as electronic loads, may be used if it can be shown that the source does not cause results that are different than would be obtained with passive resistors, inductors, and capacitors.

All AC loads shall be rated for and adjustable to all test conditions. The equations for Q_f are based upon an ideal parallel RLC circuit. For this reason, non-inductive resistors, low loss (high Q_f) inductors, and capacitors with low effective series resistance and effective series inductance shall be utilized in the test circuit. Iron core inductors, if used, shall not exceed a current THD of 2 % when operated at nominal voltage. Load components should be conservatively rated for the voltage and power levels expected. Resistor power ratings should be chosen so as to minimize thermally-induced drift in resistance values during the course of the test.

Real and reactive power should be calculated (using the measurements provided in Table 1) in each of the R, L and C legs of the load so that these parasitic parameters (and parasitics introduced by variacs or autotransformers) are properly accounted for when calculating Q_f.

6 Test for single or multi-phase inverter

6.1 Test procedure

The following test is designed for EUT consisting of a single or multi-phase inverter[1]. The test uses an RLC load, resonant at the EUT nominal frequency (50 Hz or 60 Hz) and matched to the EUT output power. For multi-phase EUT, the load shall be balanced across all phases and the switch S1 as in Figure 1 shall open all phases[2]. This test shall be performed with the EUT conditions as in Table 5, where power and voltage values are given as a percent of EUT full output rating.

EUT settings for voltage and frequency trip parameters (magnitude and timing) can affect the measured run-on time. Passing this test verifies that the unit will provide adequate islanding protection for the settings tested as well as for tighter settings (e.g., an EUT that passes the

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[1] Annex B describes the test for independent islanding detection device (relay).

[2] A loss of one or two phases in three-phase system is not considered an islanding phenomenon.

test with frequency trip settings of ± 1,5 Hz of nominal should also trip within the maximum measured run-on time for settings of, say, ± 0,5 Hz.) Conversely, when adjusted to settings outside of those tested, the EUT may experience extended run-on times. Frequency settings of ±1,5 Hz around nominal frequency and voltage settings of ±15 % around nominal voltage, for the purposes of this test procedure, should be wide enough to address the majority of utility requirements. Note that as trip settings are widened, more aggressive active anti-islanding schemes may be required that could negatively impact power quality.

Table 5 – Test conditions

Condition	**EUT output power, P_{EUT}**	**EUT input voltage[3)]**	**EUT trip settings[4)]**
A	Maximum[1)]	>90 % of rated input voltage range	Manufacturer specified voltage and frequency trip settings
B	50 % – 66 % of maximum	50 % of rated input voltage range, ±10 %	Set voltage and frequency trip settings to nominal values
C	25 % – 33 %[2)] of maximum	<10 % of rated input voltage range	Set voltage and frequency trip settings to nominal values

[1)] Maximum EUT output power condition should be achieved using the maximum allowable input power. Actual output power may exceed nominal rated output.

[2)] Or minimum allowable EUT output level if greater than 33 %.

[3)] Based on EUT rated input operating range. For example, If range is between X volts and Y volts, 90 % of range =X + 0,9 × (Y – X). Y shall not exceed 0,8 × EUT maximum system voltage (i.e., maximum allowable array open circuit voltage). In any case, the EUT should not be operated outside of its allowable input voltage range.

[4)] The manufacturer shall specify voltage and frequency trip magnitude and trip time settings with which the unit shall be tested. The recommended settings shown below should address the majority of utility requirements.

Parameter	Magnitude	Timing s
Over voltage	115 % of nominal voltage	2
Under voltage	85 % of nominal voltage	2
Over frequency	1,5 Hz above nominal frequency	1
Under frequency	1,5 Hz below nominal frequency	1

If fast over and under voltage and frequency settings are provided, similarly extended values should also be specified by the manufacturer.

a) Determine EUT test output power, P_{EUT}, to be used from Table 5. Test conditions A, B, and C may be performed in any order convenient to testing.

b) By adjusting the DC input source, operate the EUT at the selected P_{EUT} and measure EUT reactive power output, Q_{EUT}, as follows. The utility disconnect switch S1 should be closed. With no local load connected (that is, S2 is open so that the RLC load is not connected at this time), and the EUT connected to the utility (S1 is closed), turn the EUT on and operate it at the output determined in step a). Measure the fundamental frequency (50 Hz or 60 Hz) real and reactive power flow, P_{AC} and Q_{AC}. The real power should equal P_{AC}. The reactive power, Q_{AC} measured in this step is designated Q_{EUT} in the following steps.

   NOTE EUT output for condition A is achieved by providing sufficient (excess) input power to allow unit to produce its maximum output without causing it to shutdown. Condition B is achieved by adjusting the DC input power source, if the EUT provides this mode of operation. Condition C is achieved using inverter control to limit the output power, if the EUT provides this mode of operation.

c) Turn off the EUT and open S1.

   NOTE When the load component levels are adjusted using real-time measurement of resistive, inductive, and capacitive power levels, it may be necessary to leave S1 closed.

d) Adjust the RLC circuit to have $Q_f = 1{,}0 \pm 0{,}05$[3] using the following steps:

   1) Determine the amount of inductive reactance required in the resonant RLC circuit using the relation $Q_L = Q_f \times P_{EUT} = 1{,}0 \times P_{EUT}$.

   2) Connect an inductor as the first element of the RLC circuit. Adjust the inductance to Q_L.

   3) Connect a capacitor in parallel with the inductor. Adjust the capacitive reactance so that $Q_C + Q_L = -Q_{EUT}$.

   4) Connect a resistor that results in the power consumed by the RLC circuit equaling P_{EUT}.

   NOTE Real and reactive power are calculated (using the measurements provided in Table 1) for each of the R, L and C legs of the load so that these parasitic parameters (and parasitics introduced by variacs or autotransformers) are properly accounted for when calculating Q_f.

e) Connect the RLC load configured in step d) to the EUT by closing S2. Close S1 and turn the EUT on, making certain that the power output is as determined in step a). Adjust R, L, and C as necessary to ensure that the fundamental (50 Hz or 60 Hz) component of current I_{AC} through S1 is 0,0 A with tolerance of ±1 % of the rated current of the EUT on a steady state basis in each phase.[4]

   NOTE The purpose of the procedure up to this point is to zero out the fundamental frequency components (50 Hz or 60 Hz) of real and reactive power, or to zero out the fundamental frequency component of current flow, at the utility disconnect switch. System resonance will typically generate harmonic currents in the test circuit. These harmonic currents will typically make it impossible to zero out an r.m.s. measurement of power or current flow at the disconnect switch. Because of test equipment measurement error and some impact from harmonic currents, it may be necessary to make small adjustments in the test circuit to achieve worst case islanding behavior. Step h) is performed to make these small adjustments.

f) Open the utility-disconnect switch S1 to initiate the test. Run-on time, t_R, shall be recorded as the time between the opening of switch S1 and the point at which the EUT output current drops and remains below 1 % of its rated output levels. Annex C gives some information related to the use of gate blocking signal.

g) For test condition A in Table 5 (100 %), adjust the real load and only one of the reactive load components (either capacitance, C, or inductance, L, may be chosen) to each of the load imbalance conditions shown in the shaded portion of Table 6. The values in Table 6 represent changes from the nominal values determined in steps d) and e) as a percentage of those nominal values. The values in Table 6 show the real and reactive power flow at S1 in Figure 1, with positive value denoting power flow from EUT to AC power source. After each adjustment, an island test is run and run-on time is recorded. If any of the recorded run-on times are longer than the one recorded for the rated balance condition, i.e. test f), then the non-shaded parameter combinations also require testing. If no run-on Time exceeds the one of balance condition, then this part of test sequence is deemed to be completed.

h) For test conditions B and C, adjust the only one reactive load components (either capacitance, C, or inductance, L, may be chosen) by approximately 1,0 % per test, within a total range of 95 % to 105 % of the operating point as shown in Table 7. The values in Table 7 show the reactive power flow at S1 in Figure 1, with positive value denoting power flow from EUT to AC power source. After each adjustment, an island test is run and run-on time is recorded. If run-on times are still increasing at the 95 % or 105 % points, additional 1 % increments shall be taken until run-on times begin decreasing. Test C load conditions may be achieved using inverter control to limit the output power rather than using the power supply to limit the power.

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[3] The appropriate value for Q_f was investigated using 723 measurement points in Japan. A value of Q_f was calculated as the ratio of the contract demand (kW) at the measurement point to the installed shunt capacitor (kVAr) needed to make the power factor 1,0 at that point. Based on the variety of load conditions encountered, $Q_f = 1{,}0$ appears to be suitable test condition.

[4] Certain anti-islanding algorithms will sufficiently perturb the fundamental frequency current through S1 such that the 1 % limit cannot be achieved on a continuous basis. Averaging of the r.m.s. current over a number of cycles in a manner that captures the quiescent magnitude of this current shall be utilized for the determination of matched load during this quiescent period.