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SBus – Chip and module interconnect bus

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Abstract: An input/output expansion bus with a 32- or 64-bit width is described in this standard. The SBus is designed for systems requiring a small number expansion ports. SBus Cards may be connected to a standard Sbus Connector mounted on the motherboard. SBus Devices may also be attached to the SBus directly on the system's motherboard. The dimensions of the SBus Card are 83,8 mm by 146,7 mm, making the cards appropriate for small computer systems that make extensive use of highly integrated circuits. The SBus Cards are designed to be installed in a plane parallel to the system's motherboard as mezzanine cards. They are designed to provide connections for devices external to the computer system through an exposed back panel. The form factor is useful in Futurebus+, VMEbus, desktop computers, and similar applications. The SBus has the capability of transferring data at rates up to 168 Mbytes/s, depending on the implementation options selected.

SBus Cards may either serve as Masters on the bus, providing all virtual address information as well as the data to be transferred, or they may serve as Slaves on the bus, providing data transfer according to the requirements of some other SBus Master. The SBus Master for a data transfer is selected by an arbitration process managed by the single SBus Controller on the SBus. The SBus Controller provides a virtual to physical address translation service.

Keywords: I/O bus, SBus, SBus Card, Standard for Boot Firmware.

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FOREWORD

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INTRODUCTION

(This introduction is not a normative part of ISO/IEC 15205:2000, but is included for information only.)

This IEEE standard documents the implementation of the popular SBus interface. The SBus, originally developed and documented by Sun Microsystems as an I/O expansion bus, uses a standard form factor SBus Card that is a suitable size for the use of VLSI circuits in small computers. It has a high bandwidth and is capable of data transfer 8, 16, 32, or 64 bits in width. This standard includes the set of functionality originally documented by the *SBus Specification B.0* (Sun Microsystems Part #800.5922-10, Revision A, December 1990) and clarifies, corrects, and extends that functionality as required. The IEEE P1275 Working Group is developing a standard for boot firmware, which will define and document the initialization and boot interface for SBus Cards.

Special thanks are due to Bob Snively (P1496 Working Group draft technical editor) for the many hours spent in converting this document from the original *SBus Specification B.0* and editing it into its final form. Also deserving of thanks are Jim Lyle (P1496 Working Group vice Chair), Barbara Vance (P1496 Working Group former Secretary), Bob Gianni (P1496 Working Group Secretary), and Steve Hix (P1496 draft document editor) for their support in the Committee work and the generation of this document.

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SBus – CHIP AND MODULE INTERCONNECT BUS

1 General

1.1 Scope and object

SBus is a high performance computer I/O interface for connecting integrated circuits and SBus Cards to a computer system motherboard. This standard defines the mechanical, electrical, environmental, and protocol requirements for the design of SBus Cards and the computer system motherboard that supports those cards.

Every SBus Card shall implement appropriate self-descriptive and initialization firmware using FCode, which is similar to the Forth programming language. The details of this firmware standard are beyond the scope of this standard.[1)] In addition, other software interfaces may be used for communication with SBus Cards.

SBus is intended to provide a high performance I/O bus interface with a small mechanical form factor. The small size, high levels of integration, and low power usage of SBus Cards enable them to be used in laptop computers, compact desktop computers, and other applications requiring similar characteristics. SBus Cards are mounted in a plane parallel to the motherboard of the computer system, allowing the computer system to have a low profile. SBus is not designed as a general purpose backplane bus.

SBus allows transfers to be in units of 8, 16, 32, or 64 bits. Burst transfers are allowed to further improve performance. SBus allows a number of SBus Master devices to arbitrate for access to the bus. The chosen SBus Master provides a 32-bit virtual address which the SBus Controller maps to the selection of the proper SBus Slave and the development of the 28-bit physical address for that Slave. The selected SBus Slave then performs the data transfers requested by the SBus Master. Simple SBus Cards may be designed to operate solely as Slaves on the SBus.

1.2 Normative references

The following normative documents contain provisions which, through reference in this text, constitute provisions of this International Standard. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based on this International Standard are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. For undated references, the latest edition of the normative document referred to applies. Members of IEC and ISO maintain registers of currently valid International Standards.

IEEE Std 1275:1994, IEEE Standard for Boot (Initialization Configuration) Firmware: Core Requirements and Practices[2)]

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1) A firmware interface standard is under consideration.

2) IEEE publications are available from the Institute of Electrical and Electronics Engineers, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331, USA (standards.ieee.org/).

2 Definitions, usage of special terms, acronyms, and editorial conventions

2.1 Definitions

For the purposes of this standard the following definitions apply.

2.1.1
assert
a) for a single signal: to drive a signal to the one (1), or asserted, logic state.
b) for a set of parallel signals of the same function: to place the desired logic state pattern on the bus, which may include both one and zero values

2.1.2
byte
set of eight bit-parallel signals corresponding to binary digits operated on as a unit

The most significant bit carries index value 7 and the least significant bit carries index value 0.

2.1.3
byte Slave
SBus Slave having a data path only through bits D[31:24] of the data bus

2.1.4
Bus Sizing
the dynamic modification of the data transfer width to meet the SBus Slave's bus width requirements [see 5.4.6]

2.1.5
CLK
a fixed-frequency clock signal; the main SBus timing signal

2.1.6
clock cycle
one period of the CLK signal, beginning with the rising edge of the signal and ending on the following rising edge of the signal

2.1.7
Controller
see **SBus Controller**

2.1.8
central processing unit (CPU)
describes that part of a computer that does the primary computational functions; loosely describes the computer system other than connected input and output devices

2.1.9
double-word
eight bytes or 64 bits operated on as a unit.

The most significant byte carries index value 0 and the least significant byte carries index value 7.

2.1.10
half-word
two bytes or 16 bits operated on as a unit

The most significant byte carries index value 0 and the least significant byte carries index value 1.

2.1.11
half-word Slave
an SBus Slave having a data path only through bits D[31:16] of the data bus

2.1.12
high (H) level
a signal voltage within the more positive (less negative) of the two ranges of logic levels chosen to represent the logic states

2.1.13
holding amplifier
receiver circuit incorporating feedback that maintains the present input logic level in the absence of any other drive signals on the signal line

2.1.14
logic state
one of two possible abstract states that may be taken on by a binary logic variable
See **one, zero, assert, negate, signal state**.

2.1.15
logic level
any level within one of two non-overlapping ranges of values of voltage used to represent the logic states
See **high, low**.

2.1.16
low (L) level
a signal voltage within the more negative (less positive) of the two ranges of logic levels chosen to represent the logic states

2.1.17
mandatory
The referenced item is required to claim compliance with this standard.

2.1.18
Master
See **SBus Master**.

2.1.19
motherboard
the printed circuit board on which an SBus Card is mounted through the connectors specified by this standard

2.1.20
negate
to drive a signal or a parallel set of signals to the zero logic state

2.1.21
odd parity
within a field or set of fields, an odd number of bits having the logical state of one; the exclusive-OR of all the bits being checked has the value of 1

2.1.22
one ("1")
a true logic state or a true condition of a variable

2.1.23
optional
The referenced item is not required to claim compliance with this standard. Implementation of an optional item should be as defined in this standard.

2.1.24
reserved
the term used for signals, bits, fields, and code values that are set aside for future standardization

2.1.25
SBus
a) the correct spelling of the noun describing the bus defined by this standard
b) the name for the Chip and Module Interconnect Bus described by this standard

2.1.26
SBus Card
a physical printed circuit assembly that conforms to the single-width or double-width mechanical specifications; meets the connector, power, and signal assignment requirements of this standard and contains one or more SBus Devices

2.1.27
SBus Controller
the SBus Device that performs all the centralized services for the SBus, including bias circuitry, arbitration, and address translation for SBus Masters, and selection of and time-outs for SBus Slaves

2.1.28
SBus cycle
one complete operation on the SBus, consisting of a set of phases beginning with an optional Arbitration Phase and progressing through the optional Translation Phase, the optional Extended Transfer Information Phase, and the Transfer Phase

2.1.29
SBus Device
a set of circuitry complying with the electrical and protocol requirements of the SBus and properly implementing all the signals of the SBus

An SBus Device may reside on the computer motherboard or it may be on an SBus Card. See **SBus Controller, SBus Master, SBus Slave**.

2.1.30
SBus Master
the SBus Device that requests data transfers to be performed by an SBus Slave

2.1.31
SBus Master port
in an SBus Device that combines both an SBus Master and an SBus Slave, the circuitry that is associated with the SBus Master

2.1.32
SBus Slave
the SBus Device providing the function of performing the data transfers requested by an SBus Master; the address space for the data transfers may contain data, control registers, or sense registers

2.1.33
SBus Slave port
in an SBus Device that combines both an SBus Master and an SBus Slave, the circuitry that is associated with the SBus Slave

2.1.34
SBus Slot
the location on a computer motherboard in which an SBus Card may be installed

The SBus Slot has the connector, the electrical characteristics, and the physical volumes and dimensions that are required by this standard.

2.1.35
SBus Specification
SBus Specification B.0 [B1][1)], an earlier specification of SBus, now superseded by IEEE Std 1496

2.1.36
SBus standard
IEEE Std 1496, IEEE Standard for a Chip and Module Interconnect Bus: SBus

2.1.37
SBus System
a computer system containing a motherboard with at least an SBus Controller and some combination of zero or more SBus Slots which may be populated with SBus Cards

The SBus System may additionally have SBus Devices integrated on the motherboard. The SBus System includes the electronic, powering, cooling, and mechanical support functions required by the installed SBus Devices and SBus Slots.

2.1.38
signal assertion

a) the act of driving a signal to the true state

b) the act of driving a bus of signals to the correct pattern of ones and zeros

2.1.39
signal negation
the act of driving a signal to the false state

2.1.40
signal release
the act of removing electronic drive to a signal thereby placing the driver in a high-impedance condition

Release of an SBus signal will leave the SBus signal in its last state unless the signal is specified to have bias circuits attached that return the signal to a specified state.

2.1.41
signal state
logic state

2.1.42
Slave
See **SBus Slave**.

[1)] The numbers in brackets preceded by the letter B correspond to those of the bibliography in annex A.

2.1.43
word
four bytes or 32 bits operated on as a unit

The most significant byte carries index value 0 and the least significant byte carries the index value 3.

2.1.44
zero
a false logic state or a false condition of a variable

2.2 Usage of special terms

The use of special terms in this standard is explained here to prevent possible confusion:

2.2.1
shall
used when stating mandatory requirements of the standard

2.2.2
should
used when stating recommendations that are understood to be advisory

2.2.3
may
used to indicate optional directives or features

2.3 Acronyms

CPU central processing unit
LSB least significant bit
MMU memory management unit
MSB most significant bit

2.4 Editorial conventions

The following editorial conventions are used in this standard.

2.4.1 Signal names

A signal name followed by a number range in square brackets represents a set of logically related signals. The first number in the range indicates the most significant bit. As an example, D[31:0] describes the 32 bits of the data bus signals, with bit 31 being the most significant bit and bit 0 being the least significant bit.

An asterisk is appended to a signal name to indicate that its asserted or 1 state is present when the signal line's voltage is at its more negative logic level. The absence of an asterisk indicates that the signal is asserted or "1" when the signal line's voltage is at its more positive logic level. As an example, SEL* is asserted or "1" when the signal is at its more negative logic level.

2.4.2 Numbers

Values of signal names, including the value of a range of logically related signals grouped by a bracket, will be indicated as binary values with a binary character for each signal in the range. As an example, the notation PA[2:0] = 110 indicates that PA[2] has a 1 binary value, PA[1] has a 1 binary value, and that PA[0] has a 0 binary value.