Designation: F996 – 11 (Reapproved 2018)

Standard Test Method for Separating an Ionizing Radiation-Induced MOSFET Threshold Voltage Shift Into Components Due to Oxide Trapped Holes and Interface States Using the Subthreshold Current–Voltage Characteristics[1]

This standard is issued under the fixed designation F996; the number immediately following the designation indicates the year of original adoption or, in the case of revision, the year of last revision. A number in parentheses indicates the year of last reapproval. A superscript epsilon (ε) indicates an editorial change since the last revision or reapproval.

1. Scope

1.1 This test method covers the use of the subthreshold charge separation technique for analysis of ionizing radiation degradation of a gate dielectric in a metal-oxide-semiconductor-field-effect transistor (MOSFET) and an isolation dielectric in a parasitic MOSFET.[2,3,4] The subthreshold technique is used to separate the ionizing radiation-induced inversion voltage shift, ΔV_{INV} into voltage shifts due to oxide trapped charge, ΔV_{ot} and interface traps, ΔV_{it}. This technique uses the pre- and post-irradiation drain to source current versus gate voltage characteristics in the MOSFET subthreshold region.

1.2 Procedures are given for measuring the MOSFET subthreshold current-voltage characteristics and for the calculation of results.

1.3 The application of this test method requires the MOSFET to have a substrate (body) contact.

1.4 Both pre- and post-irradiation MOSFET subthreshold source or drain curves must follow an exponential dependence on gate voltage for a minimum of two decades of current.

1.5 The values stated in SI units are to be regarded as standard. No other units of measurement are included in this standard.

1.6 *This standard does not purport to address all of the safety concerns, if any, associated with its use. It is the responsibility of the user of this standard to establish appropriate safety, health, and environmental practices and determine the applicability of regulatory limitations prior to use.*

1.7 *This international standard was developed in accordance with internationally recognized principles on standardization established in the Decision on Principles for the Development of International Standards, Guides and Recommendations issued by the World Trade Organization Technical Barriers to Trade (TBT) Committee.*

2. Referenced Documents

2.1 *ASTM Standards:*[5]

E666 Practice for Calculating Absorbed Dose From Gamma or X Radiation

E668 Practice for Application of Thermoluminescence-Dosimetry (TLD) Systems for Determining Absorbed Dose in Radiation-Hardness Testing of Electronic Devices

E1249 Practice for Minimizing Dosimetry Errors in Radiation Hardness Testing of Silicon Electronic Devices Using Co-60 Sources

E1894 Guide for Selecting Dosimetry Systems for Application in Pulsed X-Ray Sources

3. Terminology

3.1 *Definitions of Terms Specific to This Standard:*

3.1.1 *anneal conditions*—the current and/or voltage bias and temperature of the MOSFET in the time period between irradiation and measurement.

3.1.2 *doping concentration*— *n*- or *p*-type doping, is the concentration of the dopant in the MOSFET channel region adjacent to the oxide/silicon interface.

[1] This test method is under the jurisdiction of ASTM Committee F01 on Electronics and is the direct responsibility of Subcommittee F01.11 on Nuclear and Space Radiation Effects.

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[2] McWhorter, P. J. and P. S. Winokur, "Simple Technique for Separating the Effects of Interface Traps and Trapped Oxide Charge in MOS Transistors," *Applied Physics Letters*, Vol 48, 1986, pp. 133–135.

[3] DNA-TR-89-157, Subthreshold Technique for Fixed and Interface Trapped Charge Separation in Irradiated MOSFETs, available from National Technical Information Service, 5285 Port Royal Rd., Springfield, VA 22161.

[4] Saks, N. S., and Anacona, M. G., "Generation of Interface States by Ionizing Radiation at 80K Measured by Charge Pumping and Subthreshold Slope Techniques," *IEEE Transactions on Nuclear Science*, Vol NS–34 , No. 6, 1987, pp. 1348–1354.

[5] For referenced ASTM standards, visit the ASTM website, www.astm.org, or contact ASTM Customer Service at service@astm.org. For *Annual Book of ASTM Standards* volume information, refer to the standard's Document Summary page on the ASTM website.

3.1.3 *Fermi level*—this value describes the top of the collection of electron energy levels at absolute zero temperature.

3.1.4 *intrinsic Fermi level*—the energy level that the Fermi level has in the absence of any doping.

3.1.5 *inversion current, I_{INV}*—the MOSFET channel current at a gate-source voltage equal to the inversion voltage.

3.1.6 *inversion voltage, V_{INV}*—the gate-source voltage corresponding to a surface potential of $2\varphi_B$.

3.1.7 *irradiation biases*—the biases on the gate, drain, source, and substrate of the MOSFET during irradiation.

3.1.8 *midgap current, I_{MG}*—the MOSFET channel current at a gate-source voltage equal to the midgap voltage.

3.1.9 *midgap voltage, V_{MG}*—the gate-source voltage corresponding to a surface potential of φ_B.

3.1.10 *oxide thickness, t_{ox}*—the thickness of the oxide of the MOSFET under test.

3.1.11 *potential, φ_B*—the potential difference between the Fermi level and the intrinsic Fermi level.

3.1.12 *subthreshold swing*—the change in the gate-source voltage per change in the log source or drain current of the MOSFET channel current below the inversion current. The value of the subthreshold swing is expressed in V/decade (of current).

3.1.13 *surface potential, φ_s*—the potential at the MOSFET semiconductor surface measured with respect to the intrinsic Fermi level.

4. Summary of Test Method

4.1 The subthreshold charge separation technique is based on standard MOSFET subthreshold current-voltage characteristics. The subthreshold drain or source current at a fixed drain to source voltage, V_{DS}, is measured as a function of gate voltage from the leakage current (or limiting resolution of the measurement apparatus) through inversion. The drain current and gate voltage are related by $I_D \alpha\ 10^{V_G}$. When plotted as log I_D versus V_G, the linear *I-V* characteristic can be extrapolated to a calculated midgap current, I_{MG}. By comparing the pre- and post-irradiation characteristics, the midgap voltage shift, ΔV_{MG} can be determined. The value of ΔV_{MG} is equal to ΔV_{ot}, which is the voltage shift due to oxide trapped charge. The difference between the inversion voltage shift, ΔV_{INV}, and ΔV_{MG} is equal to ΔV_{it}, which is the voltage shift due to interface traps. This procedure is shown in Fig. 1 for a *p*-channel MOSFET.

5. Significance and Use

5.1 The electrical properties of gate and field oxides are altered by ionizing radiation. The method for determining the dose delivered by the source irradiation is discussed in Practices E666, E668, E1249, and Guide E1894. The time dependent and dose rate effects of the ionizing radiation can be determined by comparing pre- and post-irradiation voltage shifts, ΔV_{ot} and ΔV_{it}. This test method provides a means for evaluation of the ionizing radiation response of MOSFETs and isolation parasitic MOSFETs.

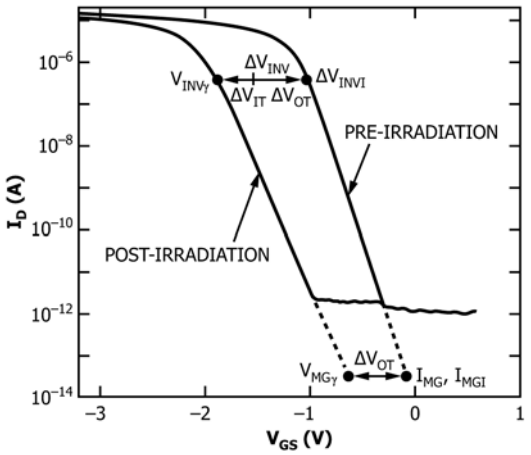

FIG. 1 Determination of Radiation Induced Voltage Shift for *p*-Channel MOSFET

5.2 The measured voltage shifts, ΔV_{ot} and ΔV_{it}, can provide a measure of the effectiveness of processing variations on the ionizing radiation response.

5.3 This technique can be used to monitor the total-dose response of a process technology.

6. Interferences

6.1 *Temperature Effects*—The subthreshold drain current varies as the exponential of $q\varphi_B/kT$, and other terms which vary as a function of temperature. Therefore, the temperature of the measurement should be controlled to within ± 2°C, since the technique requires a comparison of pre- and post-irradiation data. At cryogenic temperatures, this test method may give misleading results.[4]

6.2 *Floating Body (Kink) Effects*—Floating body effects occur in MOSFETs without body (substrate) ties. This test method should not be applied to a MOSFET without a substrate or substrate/source contact.

6.3 *Short Channel Effects*—To minimize drain voltage dependence on the subthreshold curve, a small drain measurement voltage is recommended but not necessary.

6.4 *Leakage Current*—Because the MOSFET midgap current is below the capabilities of practical current-voltage measurement instrumentation, extrapolation of the subthreshold swing is required for the determination of a MOSFET midgap voltage. Extrapolation of ideal linear MOSFET subthreshold current-voltage characteristics is unambiguous, because of the constant subthreshold swing. An example of near ideal subthreshold characteristics is given in Fig. 2, where the subthreshold current swing is relatively constant between 10^{-11} and 10^{-6} A. Nonideal subthreshold characteristics, that are aberrations from the theoretical linear subthreshold swing, can complicate the subthreshold current swing extrapolation to the midgap voltage. For subthreshold characteristics that have multiple subthreshold swings, the value of the midgap voltage would be dependent on the values of the subthreshold current from which the extrapolation is made. Nonideal subthreshold

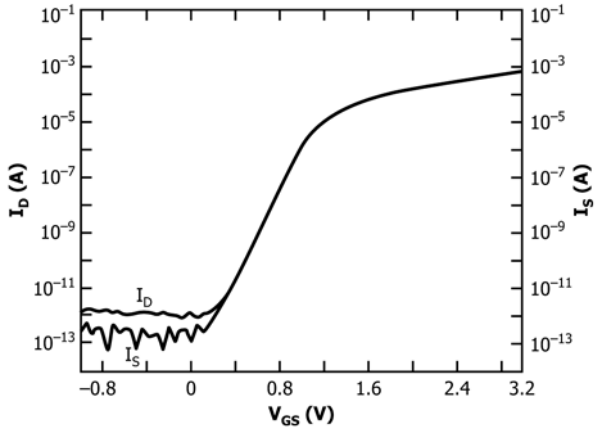

FIG. 2 Near Ideal Subthreshold Characteristics from an *n*-Channel Transistor

characteristics are caused by MOSFET leakage currents that can be either independent of, or a function of, gate-source voltage.

6.4.1 *Junction Leakage Current*—This leakage current is from the drain to the substrate and is independent of gate-source voltage. Junction leakage current masks the actual MOSFET channel subthreshold current below the leakage current level. Junction leakage current is easily distinguished from the channel subthreshold current as is shown in Fig. 2 by the flat section of the drain current, I_D, below 10^{-11}A. This figure also shows the advantage of using the source current, I_S, for extrapolation. The source current is not affected by junction leakage so that a measure of the MOSFET channel current is obtained to the instrumentation noise level. However, if there is not a separate source and substrate contact (for example, power MOSFETs), the drain current must be used. Only the part of the subthreshold curve above the junction leakage or instrumentation noise level should be used for extrapolation. A minimum of two decades of source or drain current above the leakage or noise is required for application of this test method.

6.4.2 *Gate Leakage*—Gate leakage can be any combination of leakage from the gate to source, drain, or substrate. Typically this leakage will be a function of the gate-source voltage. If gate leakage is greater than 1.0 μA for any gate-source voltage, the test method should not be applied. Gate leakages less than 1.0 μA can still cause nonideal subthreshold characteristics. The minimum value of the subthreshold source or drain current used for extrapolation to the midgap voltage must be above any changes in the subthreshold swing that can be attributed to gate leakage. Plotting the log of the gate leakage along with log source and drain current on the same graph, will aid in the determination of gate leakage effects on the drain and source subthreshold swing.

6.4.3 *Edge Leakage Current*—Most microcircuit MOSFETs use an open geometry layout so that ionizing radiation induced drain to source leakage can occur in *n*-channel devices outside of the intentional MOSFET channel. The effect of this edge leakage on the subthreshold swing is dependent on the aspect ratios and threshold voltages of the intentional and parasitic MOSFETs. The aspect ratio of the parasitic MOSFET would usually be much smaller than a standard width MOSFET layout. Thus, when the MOSFET channel is in strong inversion, the channel current will typically dominate. However, as the channel current is reduced, edge leakage can go from a minimal fraction to dominating the measured drain or source current if the parasitic MOSFET inversion voltage is less than the intentional MOSFET. This effect can be observed in the measured subthreshold characteristics as a deviation from the ideal linear subthreshold curve that is a function of the gate-source voltage. Examples of parasitic MOSFET induced deviations from the ideal linear subthreshold swing are given in Fig. 3 and Fig. 4. In Fig. 3, the subthreshold swing changes from the initial swing near inversion to a much larger mV/decade swing. In Fig. 4, a more pronounced deviation is shown. The section of the subthreshold curve that should be used for extrapolation to the midgap voltage is shown in both figures. The upper section of the subthreshold curve above the lower current level deviations was used. Any lower current change in the subthreshold swing from the initial subthreshold swing below strong inversion should be considered a parasitic MOSFET induced deviation. Only the part of the subthreshold curve above this deviation should be used for extrapolation as is shown in Fig. 3 and Fig. 4. Some *n*-channel MOSFETs may have post-irradiation edge leakage sufficiently large to prevent any observation of a subthreshold swing. The subthreshold charge separation technique cannot be applied to these samples. A minimum of two decades of source or drain current above any subthreshold swing deviation is required for application of this test method. Open and closed (annular) geometry layouts can be used to separate edge leakage current from the MOSFET channel current.

6.4.4 *Backchannel and Sidewall Leakage in a SOI MOSFET*—In a silicon-on-insulator (SOI) MOSFET, the backchannel leakage arises from a parasitic MOSFET located at the interface between the epitaxial silicon and the insulator. Sidewall leakages arise from the parasitic MOSFET formed at the edges of the intentional MOSFET. These parasitics distort the subthreshold curve in the same manner as described in 6.4.3.

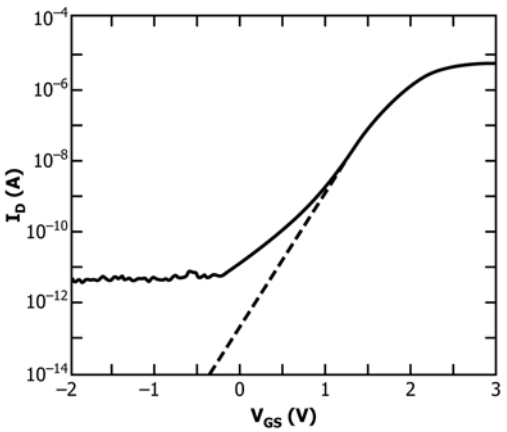

FIG. 3 Example of a Parasitic MOSFET Induced Deviation From the Ideal Linear Subthreshold Swing