Designation: F1192 – 11 (Reapproved 2018)

Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices [1]

This standard is issued under the fixed designation F1192; the number immediately following the designation indicates the year of original adoption or, in the case of revision, the year of last revision. A number in parentheses indicates the year of last reapproval. A superscript epsilon (ε) indicates an editorial change since the last revision or reapproval.

This standard has been approved for use by agencies of the U.S. Department of Defense.

1. Scope

1.1 This guide defines the requirements and procedures for testing integrated circuits and other devices for the effects of single event phenomena (SEP) induced by irradiation with heavy ions having an atomic number $Z \geq 2$. This description specifically excludes the effects of neutrons, protons, and other lighter particles that may induce SEP via another mechanism. SEP includes any manifestation of upset induced by a single ion strike, including soft errors (one or more simultaneous reversible bit flips), hard errors (irreversible bit flips), latchup (persistent high conducting state), transients induced in combinatorial devices which may introduce a soft error in nearby circuits, power field effect transistor (FET) burn-out and gate rupture. This test may be considered to be destructive because it often involves the removal of device lids prior to irradiation. Bit flips are usually associated with digital devices and latchup is usually confined to bulk complementary metal oxide semiconductor, (CMOS) devices, but heavy ion induced SEP is also observed in combinatorial logic programmable read only memory, (PROMs), and certain linear devices that may respond to a heavy ion induced charge transient. Power transistors may be tested by the procedure called out in Method 1080 of MIL STD 750.

1.2 The procedures described here can be used to simulate and predict SEP arising from the natural space environment, including galactic cosmic rays, planetary trapped ions, and solar flares. The techniques do not, however, simulate heavy ion beam effects proposed for military programs. The end product of the test is a plot of the SEP cross section (the number of upsets per unit fluence) as a function of ion LET (linear energy transfer or ionization deposited along the ion's path through the semiconductor). This data can be combined with the system's heavy ion environment to estimate a system upset rate.

1.3 Although protons can cause SEP, they are not included in this guide. A separate guide addressing proton induced SEP is being considered.

1.4 The values stated in SI units are to be regarded as standard. No other units of measurement are included in this standard.

1.5 *This standard does not purport to address all of the safety concerns, if any, associated with its use. It is the responsibility of the user of this standard to establish appropriate safety, health, and environmental practices and determine the applicability of regulatory limitations prior to use.*

1.6 *This international standard was developed in accordance with internationally recognized principles on standardization established in the Decision on Principles for the Development of International Standards, Guides and Recommendations issued by the World Trade Organization Technical Barriers to Trade (TBT) Committee.*

2. Referenced Documents

2.1 *Military Standard:*[2]

750 Method 1080

3. Terminology

3.1 *Definitions of Terms Specific to This Standard:*

3.1.1 *DUT*—device under test.

3.1.2 *fluence*—the flux integrated over time, expressed as ions/cm^2.

3.1.3 *flux*—the number of ions/s passing through a one cm^2 area perpendicular to the beam (ions/cm ^{2}-s).

3.1.4 *LET*—the linear energy transfer, also known as the stopping power dE/dx, is the amount of energy deposited per unit length along the path of the incident ion, typically normalized by the target density and expressed as MeV-cm^2/mg.

3.1.4.1 *Discussion*—LET values are obtained by dividing the energy per unit track length by the density of the irradiated medium. Since the energy lost along the track generates

[1] This guide is under the jurisdiction of ASTM Committee E10 on Nuclear Technology and Applications and is the direct responsibility of Subcommittee E10.07 on Radiation Dosimetry for Radiation Effects on Materials and Devices.

Current edition approved March 1, 2018. Published April 2018. Originally approved in 1988. Last previous edition approved in 2011 as F1192–11. DOI: 10.1520/F1192-11R18.

[2] Available from Standardization Documents Order Desk, Bldg. 4, Section D, 700 Robbins Ave., Philadelphia, PA 19111–5094.

electron-hole pairs, one can also express LET as charge deposited per unit path length (for example, picocoulombs/micron) if it is known how much energy is required to generate an electron-hole pair in the irradiated material. (For silicon, 3.62 eV is required per electron-hole pair.)

A correction, important for lower energy ions in particular, is made to allow for the loss of ion energy after it has penetrated overlayers above the device sensitive volume. Thus the ion's energy, E, at the sensitive volume is related to its initial energy, E_O, as:

$$E_s = E_o - \int_o^{(t/\cos\theta)} \left(\frac{dE(x)}{dx} \right) dx$$

where t is the thickness of the overlayer and θ is the angle of the incident beam with respect to the surface normal. The appropriate LET would thus correspond to the modified energy, E.

A very important concept, but one which is by no means universally true, is the *effective LET*. The effective LET applies for those soft error mechanisms where the device susceptibility depends, in reality, on the charge deposited within a sensitive volume that is thin like a wafer. By equating the charge deposited at normal incidence to that deposited by an ion with incident angle θ, we obtain:

$$\text{LET(effective)} = \text{LET(normal)}/\cos\theta \quad \theta < 60°$$

Because of this relationship, one can sometimes test with a single ion at two different angles to correspond to two different (effective) LETs. Note that the effective LET at high angles may not be a realistic measure (see also 6.6). Note also that the above relationship breaks down when the lateral dimensions of the sensitive volume are comparable to its depth, as is the case with VLSI and other modern high density ICs.

3.1.5 *single event burnout*—SEB (also known as SEBO) may occur as a result of a single ion strike. Here a power transistor sustains a high drain-source current condition, which usually culminates in device destruction.

3.1.6 *single event effects*—SEE is a term used earlier to describe many of the effects now included in the term SEP.

3.1.7 *single event gate rupture*—SEGR (also known as SEGD) may occur as a result of a single ion strike. Here a power transistor sustains a high gate current as a result of damage of the gate oxide.

3.1.8 *single event functionality interrupt*—SEFI may occur as a result of a single ion striking a special device node, used for an electrical functionality test.

3.1.9 *single event hard fault*—often called hard error, is a permanent, unalterable change of state that is typically associated with permanent damage to one or more of the materials comprising the affected device.

3.1.10 *single event latchup*—SEL is an abnormal low impedance, high-current density state induced in an integrated circuit that embodies a parasitic pnpn structure operating as a silicon controlled rectifier.

3.1.11 *single event phenomena*—SEP is the broad category of all semiconductor device responses to a single hit from an energetic particle. This term would also include effects induced by neutrons and protons, as well as the response of power transistors—categories not included in this guide.

3.1.12 *single event transients, (SET)*—SET's are SE-caused electrical transients that are propagated to the outputs of combinational logic IC's. Depending upon system application of these combinational logic IC's, SET's can cause system SEU.

3.1.13 *single event upset, (SEU)*—comprise soft upsets and hard faults.

3.1.14 *soft upset*—the change of state of a single latched logic state from one to zero, or vice versa. The upset is "soft" if the latch can be rewritten and behave normally thereafter.

3.1.15 *threshold LET*—for a given device, the threshold LET is defined as the minimum LET that a particle must have to cause a SEU at θ = 0 for a specified fluence (for example, 10^6 ions/cm^2). In some of the literature, the threshold LET is also sometimes defined as that LET value where the cross section is some fraction of the "limiting" cross section, but this definition is not endorsed herein.

3.1.16 *SEP cross section*—is a derived quantity equal to the number of SEP events per unit fluence.

3.1.16.1 *Discussion*—For those situations that meet the criteria described for usage of an effective LET (see 3.1.4), the SEP cross section can be extended to include beams impinging at an oblique angle as follows:

$$\sigma = \frac{\text{number of upsets}}{\text{fluence} \times \cos\theta}$$

where θ = angle of the beam with respect to the perpendicularity to the chip. The cross section may have units such as cm^2/device or cm^2/bit or μm^2/bit. In the limit of high LET (which depends on the particular device), the SEP cross section will have an area equal to the sensitive area of the device (with the boundaries extended to allow for possible diffusion of charge from an adjacent ion strike). If any ion causes multiple upsets per strike, the SEP cross section will be proportionally higher. If the thin region waferlike assumption for the shape of the sensitive volume does not apply, then the SEP cross section data become a complicated function of incident ion angle. As a general rule, high angle tests are to be avoided when a normal incident ion of the same LET is available.

A limiting or asymptotic cross section is sometimes measured at high LET whenever all particles impinging on a sensitive area of the device cause upset. One can establish this value if two measurements, having a different high LET, exhibit the same cross sections.

3.2 *Abbreviations:*

3.2.1 *ALS*—advanced low power Schottky.

3.2.2 *CMOS*—complementary metal oxide semiconductor device.

3.2.3 *FET*—field effect transistor.

3.2.4 *IC*—integrated circuit.

3.2.5 *NMOS*—*n*-type-channel metal oxide semiconductor device.

3.2.6 *PMOS*—*p*-type-channel metal oxide semiconductor device.

3.2.7 *PROM*—programmable read only memory.

3.2.8 *RAM*—random access memory.

3.2.9 *VLSI*—very large scale integrated circuit.

4. Summary of Guide

4.1 The SEP test consists of irradiation of a device with a prescribed heavy ion beam of known energy and flux in such a way that the number of single event upsets or other phenomena can be detected as a function of the beam fluence (particles/cm^2). For the case where latchup is observed, a series of measurements is required in which the fluence is recorded at which latchup occurs, in order to obtain an average fluence.

4.2 The beam LET, equivalent to the ion's stopping power, *dE/dx*, (energy/distance), is a fundamental measurement variable. A full device characterization requires irradiation with beams of several different LETs that in turn requires changing the ion species, energy, or, in some cases, angle of incidence with respect to the chip surface.

4.3 The final useful end product is a plot of the upset rate or cross section as a function of the beam LET or, equivalently, a plot of the average fluence to cause upset as a function of beam LET. These comments presume that LET, independent of *Z*, is a determinant of SE vulnerability. In cases where charge density (or charge density and total charge) per unit distance determine device response to SEs, results provided solely in terms of LET may be incomplete or inaccurate, or both.

4.4 *Test Conditions and Restrictions*—Because many factors enter into the effects of radiation on the device, parties to the test should establish and record the test conditions to ensure test validity and to facilitate comparison with data obtained by other experimenters testing the same type of device. Important factors which must be considered are:

4.4.1 *Device Appraisal*—A review of existing device data to establish basic test procedures and limits (see 8.1),

4.4.2 *Radiation Source*—The type and characteristics of the heavy ion source to be used (see 7.1),

4.4.3 *Operating Conditions*—The description of the testing procedure, electrical biases, input vectors, temperature range, current-limiting conditions, clocking rates, reset conditions, etc., must be established (see Sections 6, 7, and 8),

4.4.4 *Experimental Set-Up*—The physical arrangement of the accelerator beam, dosimetry electronics, test device, vacuum chamber, cabling and any other mechanical or electrical elements of the test (see Section 7),

4.4.5 *Upset Detection*—The basis for establishing upset must be defined (for example, by comparison of the test device response with some reference states, or by comparison of post-irradiation bit patterns with the pre-irradiation pattern, and the like (see 7.4)). Tests of heavy ion induced transients require special techniques whose extent depends on the objectives and resources of the experimenter,

4.4.6 *Dosimetry*—The techniques to be used to measure ion beam fluxes and fluence.

4.4.7 *Flux Range*—The range of heavy ion fluxes (both average and instantaneous) must be established in order to provide proper dosimetry and ensure the absence of collective effects on device response. For heavy ion SEP tests a normal flux range will be 10^2 to 10^5 ions/cm ^{2}-s. However, higher fluxes are acceptable if it can be established that dosimetry and tester limits, coincident upset effects, device heating, and the like, are properly accounted for. Such higher limits may be needed for testing future smaller geometry parts.

4.4.8 *Particle Fluence Levels*—The minimum fluence is that fluence required to establish that an observance of no upsets corresponds to an acceptable upper bound on the upset cross section with a given confidence. Sufficient fluence should be provided to also ensure that the measured number of upset events provides an upset cross section whose magnitude lies within acceptable error limits (see 8.2.7.2). In practice, a fluence of 10^7 ions/cm^2 will often meet these requirements.

4.4.9 *Accumulated Total Dose*—The total accumulated dose shall be recorded for each device. However, it should be noted that the average dose actually represents a few heavy ion tracks, <10 nm in diameter, in each charge collection region, so this dose may affect the device physics differently than a uniform (for example, gamma) dose deposition. In particular, it is sometimes observed that accumulated dose delivered by heavy ions is less damaging than that delivered with uniform dose deposition.

4.4.10 *Range of Ions*—The range or penetration depth of the energetic ions is an important consideration. An adequate range is especially crucial in detecting latchup, because the relevant junction is often buried deep below the active chip. Some test requirements specify an ion range of >30 µm. The U.C. Berkeley 88-inch cyclotron and the Brookhaven National Laboratory Van de Graaff have adequate energy for most ions, but not all. Gold data at BNL is frequently too limited in range to give consistent results when compared to nearby ions of the periodic table. Medium-energy sources, such as the K500 cyclotron at Texas A & M, easily satisfy all range requirements. High-energy machines that simulate cosmic ray energies, such as GANIL (Caen, France) and the cyclotron at Darmstadt, Germany, provide greater range.

5. Significance and Use

5.1 Many modern integrated circuits, power transistors, and other devices experience SEP when exposed to cosmic rays in interplanetary space, in satellite orbits or during a short passage through trapped radiation belts. It is essential to be able to predict the SEP rate for a specific environment in order to establish proper techniques to counter the effects of such upsets in proposed systems. As the technology moves toward higher density ICs, the problem is likely to become even more acute.

5.2 This guide is intended to assist experimenters in performing ground tests to yield data enabling SEP predictions to be made.

6. Interferences

6.1 There are several factors which need to be considered in accommodating interferences affecting the test. Each is described herein.

6.2 *Ion Beam Pile-up*—When an accelerator is being chosen to perform a SEP test, the machine duty cycle needs to be

considered. In general, the instantaneous pulsed flux arriving at the DUT or scintillation is higher than the average measured flux, and the increase is given by the inverse of the duty cycle. A calculation should be made to ensure that no more than one particle is depositing charge in the DUT or scintillator at the same time. (The time span defining the "same time" is determined by the rate at which DUT elements are reset or at which the scintillator saturates.)

6.3 *Radiation Damage:*

6.3.1 A history of previous total dose irradiations for the DUTs must be known to assist in the determination of whether prior total ionizing dose has affected the SEP response.

6.3.2 During a test, the usual fluence for heavy ion tests (10^6 to 10^7 ions/cm^2) corresponds to kilorad dose levels in the parts. Total dose accumulated during the test shall be recorded, because the radiation effects of the accumulated dose may alter the SEP effect being monitored.

6.3.3 Sustained tests over a long period of time may lead to permanent degradation of electronics components, computers, sockets, etc. Fixtures must be checked regularly for signs of radiation damage, such as high leakage currents.

6.4 *Temperature*—Latchup susceptibility and soft error cross sections increase with temperature. In addition there are special situations in which SEP susceptibility will be particularly sensitive to temperature (for example, from the temperature dependence of feedback resistors).

6.5 *Electrical Noise:*

6.5.1 *Generalized Noise*—Because of the amount of electrical noise present in the vicinity of an accelerator, careful noise reduction techniques are mandatory. Cable lengths should be as short as possible, consistent with constraints imposed by the accelerator facility lay-out.

6.5.2 The tester must interact with accelerator personnel to ensure that the accelerator power supply is free of on-line instabilities that may affect the alignment and uniformity of the beam.

6.6 *Background Radiation*—Radioactivity induced by the heavy ion tests is minimal. The tester should perform radioactivity checks of the DUT board and parts after sustained runs; however, in general, DUTs may be safely packed and transported without delay after test.

6.7 *Ion Interaction Effects:*

6.7.1 The calculation of an effective LET (see discussion in 3.1.4) hinges on the thin slab approximation of the sensitive volume, which is less likely to hold for high density, small geometry devices. This problem can be examined by investigating the device SEP response to two different ions having the same effective LET.

6.7.2 The proportion of length to width of the sensitive volume is also assumed equal to one. Rotating the device along both axes of symmetry during the test may provide a more meaningful characterization.

6.7.3 As geometries continue to scale down, the possibility of multiple bit upsets increases. Hence, the nature of the ion's radial energy deposition becomes more important and it becomes more likely that two different ions of equivalent LET do not in fact have an equal SEP effect. In addition, the effects of irradiating at an angle become much more complex when an ion track overlaps two cells. The frequency of such overlapping upsets likewise depends on the track's radial energy deposition. Use of ions having adequate range is also important. Lower energy heavy ions lose LET as they slow down by attaching electrons and also show a contraction in the width of the radial energy deposition.

7. Apparatus and Radiation Sources

7.1 *Particle Radiation Sources*—The choice of radiation sources is important. Hence source selection guidelines are given here. A test covering the full range of LET values (both high and low *Z* ions) will require an accelerator. Cost, availability, lead times, and ion/energy capabilities are all important considerations in selecting a facility for a given test. Three source types are commonly used for conducting SEP experiments, each of which has specific advantages and disadvantages (see 8.1).

7.1.1 The three source types used for heavy ion SEP measurement are as follows:

7.1.1.1 *Cyclotrons*—Cyclotrons provide the greatest flexibility of test options because they can supply a number of different ions (including alpha particles) at a finite number of different energies. The maximum available ion energy of the heavy ion machines is usually greater than the energy (2 MeV/nucleon) corresponding to the maximum LET. Hence, the ions can be selected to have adequate penetration (range) in the device.

7.1.1.2 *Van de Graaff Accelerators* —These accelerators have the important advantage of being able to pinpoint low LET thresholds of sensitive devices where lower energy, lower *Z* ions of continuously variable energies are desirable. These machines also offer a rapid change of ion species and are somewhat less expensive to operate than cyclotrons. However, because van de Graaff machines have limited energy, it may not be possible to obtain higher *Z* particles having an adequate range in some machines.

7.1.1.3 *Alpha Emitters*—Naturally occurring radioactive alpha emitters provide a limited source for screening parts that are very sensitive to SEU. Some alpha emitters (for example, americium) emit particles with a single energy so that they can be used for establishing a precise LET threshold (of the order of <1 MeV/(mg/cm^2)).

7.2 *Test Instrumentation*—The test instrumentation can be divided into two categories: (*1*) Beam delivery, characterization and dosimetry, and (*2*) Device tester (input stimulus generator and response recorder) designed to accommodate the specified devices. The details of item (*1*) above are spelled out

in 7.5.4, 7.5.5 and 7.5.6. The details of item (*2*) cannot be spelled out, but test philosophy and logic is sketched in 7.4. For information on various test instrumentation systems refer to Nichols.[3]

7.3 *Test Boards*—The DUTs will be placed on a board, often within a vacuum chamber, during the test. To reduce the number of vacuum pump downs that will be required, it is highly desirable to include sockets in the boards for several devices. The board must be remotely positionable to change from one DUT under test to another, and rotatable to permit the beam to strike the DUT at oblique angles. Tester-to-DUT card cabling should be made compatible, if needed, with the vacuum chamber bulkhead connectors to facilitate checkout prior to chamber installation.

7.4 *DUT Tester:*

7.4.1 There are many ways to design a tester/counter to measure soft errors, with special features best suited to a specified test application. However, there are certain general desirable features which any tester design should incorporate, and these will be addressed briefly.

7.4.2 Except in the simplest of special cases where a dedicated hardware tester is most desirable, the tests are performed by a computer, which exercises the DUTs directly, or alternatively makes use of an auxiliary "exerciser" or pattern operator. A tester whose design is based on the first approach, can be said to be "Computer Dominated," while the second type of design has been termed "Computer Assisted." Regardless of the test approach, the tester must be able to carry out the following operations:

7.4.2.1 Device initialization and functionality check.

7.4.2.2 Device operation while under irradiation.

7.4.2.3 Error detection and logging.

7.4.2.4 Diagnostic display in real or near-real time.

7.4.2.5 Data processing, storage and retrieval for display.

7.4.3 While an effectively infinite variety of testers can be built to function adequately in any given set of circumstances, every tester, in addition to performing the operations listed above, should possess most of the following characteristics:

7.4.3.1 Adaptability to many device types. This generally implies software control with programs written in a high-level language.

7.4.3.2 Well-defined duty factor (ratio of device "live" time to total elapsed time). Without a knowledge of the duty factor, device vulnerability cannot be quantified.

7.4.3.3 Speed of operation and high duty factor. This is especially important when tests are performed in a high particle flux. Generally, a computer-assisted tester design is implied by this characteristic.

7.4.3.4 Real-time diagnostic data display capability. Mandatory for immediate detection of anomalous test conditions and data.

7.4.3.5 Capability for some data reduction while tests are in progress. Desirable for optimization of test procedures while data are being acquired.

7.4.4 In summary, a tester will usually be of the computer-dominated or computer-assisted type. It should be programmable to accommodate a variety of device types with a minimum need for new, specialized hardware interfaces and minimum time required for reprogramming. The tester design should be sufficiently flexible to meet the changing requirements of new device technologies. Finally, the experimenter must understand the extent to which the device is being tested (its fault coverage) in order to arrive at a quantitative result. He must know what fraction of the time the device is in a SEP-susceptible mode and also what fraction of the chip's susceptible elements are omitted from testing altogether. Complex devices do not always permit easy testing access. In such cases, a thorough understanding of the untested elements must be obtained to permit extrapolation from data obtained by the test.

7.5 *Typical Cyclotron Test Set-Up:*

7.5.1 *Schematic*—A schematic overview of a typical SEP test set-up is provided in Fig. 1. The essential features are a collimated, spatially uniform beam of particles entering a vacuum chamber which may be located in an area remote (for example, behind shielded walls) from the tester/counter and dosimetry electronics. Test boards, shutters, and beam diagnostic detectors are in, or near, the vacuum chamber.

7.5.2 *Vacuum Chamber*—A typical vacuum chamber interior is shown in Fig. 2. The essential features are the beam collimators/shutters and sensors, and a rotatable and translatable board for positioning the selected DUT at the selected angle in the beam. Dosimetry may or may not be located in the vacuum chamber.

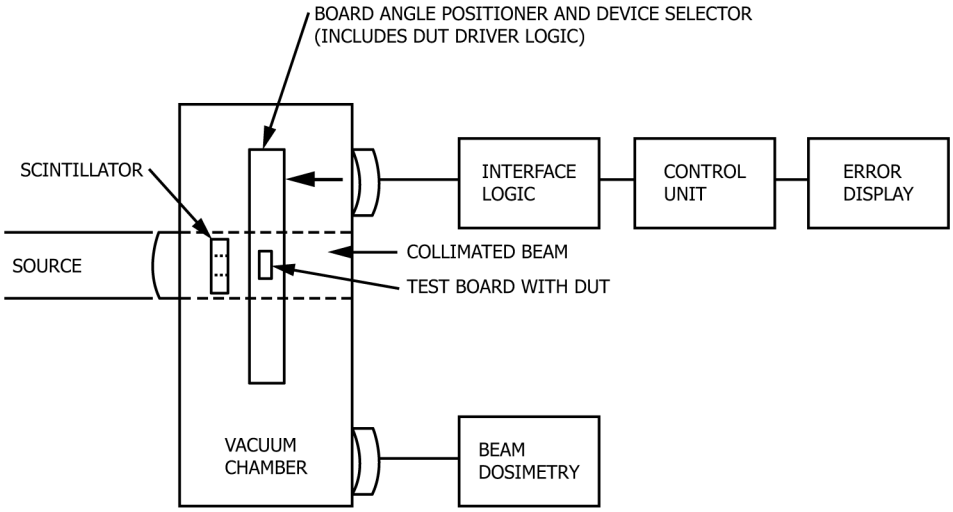
7.5.3 *DUT Board*—A typical board showing sockets for several DUTs is shown in Fig. 3, together with the associated driver logic. A device located outside the beam can be used as a reference device or sometimes one-half of a test device can be used to compare with the other half when the likelihood of both sides being hit at the same time is low.

7.5.4 *Beam Dosimetry System:*

7.5.4.1 The flux and fluence of the selected heavy ion beam may be measured by passing it through a scintillator. The beam may pass through a very thin (microns) foil whose thickness is chosen to give the proper light amplitude to correspond with the beam's LET. An alternate method is to insert an annular scintillator into the beam which admits part of the beam unimpeded onto the DUT while the outer portion is stopped by a thick scintillator. The light is then piped to a photomultiplier tube (PMT) and counted as shown in Fig. 4. The source facility typically provides the dosimetry.

7.5.4.2 The bias applied to the PMT will be increased gradually until pulses are of adequate amplitude to permit discriminator adjustment. The discriminator must reject all noise pulses and pass all pulses caused by the beam particles. The beam intensity (flux) should be kept low enough to avoid

[3] Nichols, D. K., et al, "Trends in Parts Susceptibility to Single Event Upset From Heavy Ions," *IEEE Transactions on Nuclear Science*, Vol NS-32, No. 6, December 1985, p. 4187 . (See updated addition by D. K. Nichols et al in *IEEE Transactions on Nuclear Science*, Vol NS-34, No. 6, December 1987, p. 1332, Vol NS-36, December 1989, p. 2388, Vol NS-38, December 1991 , p. 1529 , Vol NS-40, December 1993, Vol NS-42, December 1995 , *IEEE Radiation Effects Data Workshop*, December 1993, p. 1). Sections on Single Event Phenomena, *IEEE Transactions on Nuclear Science*, all December issues dating from 1979.



NOTE 1—See also Fig. 2 and Fig. 3.

FIG. 1 Typical Schematic Overview of SEP Test

pulse pile-up in the dosimetry electronics. Otherwise a measurement of the single pulse length and a calculation of the pile-up effect on the counter readout are required.

7.5.5 *Uniformity Measurement System*—Beam uniformity will first be established in a gross manner by suitable accelerator adjustments leading to a visibly uniform beam displayed on a quartz plate inside the beam tube when the accelerator is run at high fluxes. After the intensity has been reduced (usually by several orders of magnitude), the uniformity can be rapidly checked in several ways: (1) Radial uniformity by comparing beam count in two concentric circles of different areas (scintillator area versus area of solid state detector at rear), (2) Uniformity obtained by vertical motion of DUT board frame to which a horizontally mounted, position-sensitive detector is affixed, and (3) Measurement at selected points around the beam circumference. In general a 10 % variation in beam readings is deemed acceptable.

7.5.6 *Beam Energy Measurement System*—The system, shown in Fig. 5, consists of a bias supply, test pulser, surface barrier detector with collimator, preamplifier, spectroscopy amplifier, multichannel analyzer (MCA), and the radioactive calibration source. Calibration of the system is performed, using a radioactive source of known alpha particle energy. The energy spectrum can be displayed on a MCA screen. Some degradation in energy occurs between the reported energy at the source and at the DUT. In most modern facilities this instrumentation is incorporated into the beam line and the results are provided to the user in real time.

7.6 *High Energy Machine Features*—A high energy machine provides energies of several GeV per atomic mass unit more characteristic of cosmic ray energies than other sources. This fact affords simplification in some aspects of testing. There may be no need to use a vacuum chamber nor to remove lids from the devices, since beam energies are adequate to penetrate through air and the whole device structure. High energy machines may have special beams and dosimetry problems, and are unlikely to provide the same flexibility as low energy machines for changing ions and energies.

7.7 *Open Air Systems*—At appropriate beam energies open air testing can be facilitated. Performing this testing the setup will be the same as vacuum chamber testing except the vacuum feed through is not necessary.

8. Procedure

8.1 *Device Appraisal:*

8.1.1 The first step is to estimate the device SEP susceptibility by surveying existing data. From this data survey, or from information obtained from modeling studies, it may be possible to obtain an estimate of the LET (linear energy transfer) threshold for the devices to be tested. Such information can assist in the selection of ion species (and energy) with which to begin the test runs, using published values for LET for ions of various energies. Much of the SEP device test data has been published in the open literature.[3]

8.1.2 To estimate the LET threshold for a given device one can use the following approach. First look for data for devices having a similar function, technology and similar feature sizes (transistor density), irrespective of the manufacturer. If alpha particle data is available, any observed upsets would indicate a very sensitive device with a threshold LET $\leq$ 1 MeV/(mg/cm^2). If proton data is available, any upsets also show a sensitive device, probably with an LET threshold $\leq$ 6 MeV/(mg/cm^2). Any heavy ion data available also provides a very crude estimate of what might be expected for the device to be tested. If no data is available, one should assume that certain technologies and functions have a high risk for upset. For silicon devices, a rough division is given as follows:

HIGH RISK DEVICES:	LOWER RISK DEVICES:
1) Bipolar RAMs	1) Some CMOS bulk devices (except for possible latchup)
2) Low power logic (54Lxxx)	2) Some CMOS/SOS technology
3) LS and ALS (low power Schottky) logic	3) Standard power logic
4) Microprocessors and bit-slices	4) PROMs
5) NMOS, PMOS technology	5) Low speed devices
6) Dynamic RAMs	6) Devices having large feature sizes (≥10 μm)