

INTERNATIONAL STANDARD

NORME INTERNATIONALE

**Semiconductor devices - Mechanical and climatic test methods -
Part 23: High temperature operating life**

**Dispositifs à semiconducteurs - Méthodes d'essais mécaniques et climatiques -
Partie 23: Durée de vie en fonctionnement à haute température**



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INTERNATIONAL ELECTROTECHNICAL COMMISSION

**Semiconductor devices - Mechanical and climatic test methods -
Part 23: High temperature operating life**

FOREWORD

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This second edition cancels and replaces the first edition published in 2004 and Amendment 1:2011. It is based on JEDEC JESD22-A108G. It is used with permission of the copyright holder, JEDEC Solid State Technology Association. This edition constitutes a technical revision.

This edition includes the following significant technical changes with respect to the previous edition:

- a) absolute stress test definitions and resultant test durations have been updated.

The text of this International Standard is based on the following documents:

Draft	Report on voting
47/2962/FDIS	47/2983/RVD

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/publications.

A list of all parts in the IEC 60749 series, published under the general title *Semiconductor devices - Mechanical and climatic test methods*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under webstore.iec.ch in the data related to the specific document. At this date, the document will be

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1 Scope

This part of IEC 60749 specifies the test used to determine the effects of bias conditions and temperature on solid state devices over time. It simulates the device operating condition in an accelerated way and is primarily for device qualification and reliability monitoring. A form of high temperature bias life using a short duration, popularly known as "burn-in", can be used to screen for infant-mortality related failures. The detailed use and application of burn-in is outside the scope of this document.

2 Normative references

There are no normative references in this document.

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminology databases for use in standardization at the following addresses:

- IEC Electropedia: available at <https://www.electropedia.org/>
- ISO Online browsing platform: available at <https://www.iso.org/obp>

3.1

maximum operating voltage

maximum supply voltage at which a device is specified to operate in compliance with the applicable device specification or data sheet

3.2

absolute maximum rated voltage

maximum voltage that can be applied to a device, beyond which damage (latent or otherwise) is likely to occur

Note 1 to entry: It is frequently specified by device manufacturers for a specific device or technology, or both.

3.3

absolute maximum rated junction temperature

maximum junction temperature of an operating device beyond which damage (latent or otherwise) will likely occur

Note 1 to entry: It is frequently specified by device manufacturers for a specific device or technology, or both.

Note 2 to entry: Manufacturers can also specify maximum case temperatures for specific packages.

4 Test apparatus

4.1 Testing requirements

The performance of this test requires equipment that is capable of providing the particular stress conditions to which the test samples will be subjected.

4.2 Circuitry

The circuitry through which the samples will be biased shall be designed to take into account several considerations, as outlined below.

4.3 Device schematic

The biasing and operating schemes shall consider the limitations of the device and shall not overstress the devices or contribute to thermal runaway.

4.4 Power

The test circuit shall be designed to limit power dissipation such that, if a device failure occurs, excessive power will not be applied to other devices in the sample.

4.5 Device mounting

Equipment design, if required, shall provide for mounting of devices to minimize adverse effects while parts are under stress (e.g. improper heat dissipation).

4.6 Power supplies and signal sources

Instruments (such as digital voltmeters, oscilloscopes, etc.) used to set up and monitor power supplies and signal sources shall be calibrated and have good long-term stability.

4.7 Environmental chamber

The environmental chamber shall be capable of maintaining the specified temperature within a tolerance of ± 5 °C throughout the chamber while parts are loaded and unpowered.

5 Procedure

5.1 Stress requirements

The sample devices shall be subjected to the specified or selected stress conditions for the time and temperature required.

5.2 Stress duration

The bias life duration is intended to meet or exceed an equivalent field lifetime under use conditions. The duration is established based on the acceleration of the stress. The stress duration is specified by the relevant specification. Interim measurements are performed as necessary, subject to the restrictions in Clause 7.

5.3 Stress conditions

5.3.1 Stress condition application

The stress condition shall be applied continuously (except during interim measurement periods). The time spent elevating the chamber to accelerated conditions, reducing chamber conditions to room ambient and conducting the interim measurements shall not be considered a portion of the total specified test duration.