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Semiconductor devices - Generic semiconductor qualification guidelines - Part 3: Guidelines for reliability qualification plans for power semiconductor module

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IEC 63287-3 has been prepared by IEC technical committee 47: Semiconductor devices. It is an International Standard.

The text of this International Standard is based on the following documents:

Draft	Report on voting
47/3015/FDIS	47/3026/RVD

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/publications.

A list of all parts in the IEC 63287 series, published under the general title *Semiconductor devices - Generic semiconductor qualification guidelines*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under webstore.iec.ch in the data related to the specific document. At this date, the document will be

– reconfirmed,
– withdrawn, or
– revised.

INTRODUCTION

When performing qualification tests, semiconductor device vendors prepare a specific reliability test plan upon consultation with semiconductor device users in order to efficiently carry out the reliability test.

This guideline presents examples of methods for preparing test plans to determine appropriate reliability test conditions, based on the level of quality required in the operating environments of various applications of power semiconductor modules. As a target of reliability, grades have been specified for each of the following applications: automotive, industrial and consumer electronics. Based on the number of annual operating hours, use period and other parameters assumed for each grade, this guideline defines verification methods for the wear-out failure, and proposes appropriate reliability tests. This guideline defines the concept of quality assurance from early failure to wear-out failure. It also presents approaches to appropriately ensure the reliability of power semiconductor modules.

The test conditions and the acceleration factor values presented in this guideline are only examples used for setting reliability test conditions to verify a required level of quality.

NOTE Qualification tests are tests performed by power semiconductor device vendors, taking into account the quality required by the users of their products.

1 Scope

This part of IEC 63287 specifies guidelines for a reliability qualification plan for power semiconductor modules to assure reliability targets over the entire product life.

Power semiconductor modules with incorporated control circuits are excluded. Clamped packages that need external pressure for being mounted in a system are excluded, e.g. disc-type pressure pack devices.

This document is not intended for medical, military, aeronautics and astronautics-related applications.

NOTE Throughout the document, the term power semiconductor module refers to multichip semiconductor power modules as defined in 3.3.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 63287-1:2021, *Semiconductor devices - Generic semiconductor qualification guidelines - Part 1: Guidelines for IC reliability qualification*

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminology databases for use in standardization at the following addresses:

– IEC Electropedia: available at https://www.electropedia.org/

– ISO Online browsing platform: available at https://www.iso.org/obp

3.1
failure mode
classification of a fault phenomenon which causes product failure

Note 1 to entry: Disconnection, a short circuit, occasional loss, abrasion, characteristic deterioration, etc., are typical items considered as failure modes.

3.2
failure mechanism
physical, chemical or other process that results in a failure mode, which leads to a product that fails to meet functional requirements

3.3
power module
isolated or non-isolated semiconductor module with two or more semiconductor chips, according to the package outline style code “MP” specified in IEC 60191-4

Note 1 to entry: The predominantly used package body material is plastic (including epoxy) according to IEC 60191-4 and both the frame based and resin based embodiment are possible.

3.4
mode A failure
early failure with a decreasing failure rate due to extrinsic defects

3.5
mode B failure
random failure with relatively constant failure rate

Note 1 to entry: End of mode B regime limits the use period of a power semiconductor module.

3.6
mode C failure
wear-out failure with increasing failure rate due to intrinsic limitation of lifetime

3.7
bathtub curve
plot of failure rate versus time or cycles that exhibits three phases of life: infant mortality (decreasing failure rate), random failure period (relatively constant failure rate), and intrinsic wear-out (increasing failure rate)

4 Product categories and applications

4.1 Quality grade by application

Level of quality, operating hours and operating environment required for power semiconductor modules in the market are varied, depending on the application of products for which power semiconductor modules are used. As an example of a method for preparing test plans, this guideline has grouped the applications into three major grades of requirements, namely the automotive, the industrial and the consumer electronics application. For each grade, the required level of quality and its preconditions are defined, as shown in Table 1.