

TECHNICAL REPORT

**Process management for avionics - Electronic components capability in
operation -
Part 2: Semiconductor microcircuit lifetime**

get full document from standards.iteh.ai



THIS PUBLICATION IS COPYRIGHT PROTECTED

Copyright © 2026 IEC, Geneva, Switzerland

All rights reserved. Unless otherwise specified, no part of this publication may be reproduced or utilized in any form or by any means, electronic or mechanical, including photocopying and microfilm, without permission in writing from either IEC or IEC's member National Committee in the country of the requester. If you have any questions about IEC copyright or have an enquiry about obtaining additional rights to this publication, please contact the address below or your local IEC member National Committee for further information.

IEC Secretariat
3, rue de Varembe
CH-1211 Geneva 20
Switzerland

Tel.: +41 22 919 02 11
info@iec.ch
www.iec.ch

About the IEC

The International Electrotechnical Commission (IEC) is the leading global organization that prepares and publishes International Standards for all electrical, electronic and related technologies.

About IEC publications

The technical content of IEC publications is kept under constant review by the IEC. Please make sure that you have the latest edition, a corrigendum or an amendment might have been published.

IEC publications search -

webstore.iec.ch/advsearchform

The advanced search enables to find IEC publications by a variety of criteria (reference number, text, technical committee, ...). It also gives information on projects, replaced and withdrawn publications.

IEC Just Published - webstore.iec.ch/justpublished

Stay up to date on all new IEC publications. Just Published details all new publications released. Available online and once a month by email.

IEC Customer Service Centre - webstore.iec.ch/csc

If you wish to give us your feedback on this publication or need further assistance, please contact the Customer Service Centre: sales@iec.ch.

IEC Products & Services Portal - products.iec.ch

Discover our powerful search engine and read freely all the publications previews, graphical symbols and the glossary. With a subscription you will always have access to up to date content tailored to your needs.

Electropedia - www.electropedia.org

The world's leading online dictionary on electrotechnology, containing more than 22 500 terminological entries in English and French, with equivalent terms in 25 additional languages. Also known as the International Electrotechnical Vocabulary (IEV) online.

Warning! Make sure that you obtained this publication from an authorized distributor.

CONTENTS

FOREWORD	3
INTRODUCTION	5
1 Scope	6
2 Normative references	6
3 Terms, definitions and abbreviated terms	7
3.1 Terms and definitions	7
3.2 Abbreviated terms	9
4 Lifetime assessment process and method	10
4.1 General	10
4.2 Input data for the method	12
4.2.1 General	12
4.2.2 COTS semiconductor microcircuits and lifetime issues considerations	12
4.2.3 Operating and thermal conditions	12
4.3 Lifetime requirements in mission	13
4.3.1 Lifetime requirements for electronic equipment in mission	13
4.3.2 Lifetime requirement for COTS semiconductor microcircuit	13
4.4 Lifetime assessment for COTS semiconductor microcircuit	13
4.4.1 Availability of lifetime assessment by the OCM	13
4.4.2 Lifetime compliance or other alternative	14
4.4.3 Alternative approach for lifetime assessment	14
4.5 Lifetime assessment for a COTS semiconductor microcircuit processed by the OCM, based on OEM mission profile	14
4.5.1 Approach	14
4.5.2 Contact and agreement with the OCM	14
4.5.3 Custom lifetime assessment by the OCM	15
4.6 Lifetime assessment for a COTS semiconductor microcircuit processed by the OEM	15
4.6.1 Approach	15
4.6.2 Risk analysis based on physics of failure (PoF) and the component family	15
4.6.3 OCM's technical data availability and relevance	15
4.6.4 Acceleration models assessment paths	16
4.7 Lifetime calculation of COTS semiconductor microcircuit in mission	17
4.8 Lifetime compliance of COTS semiconductor microcircuit in mission	17
4.9 Situation reconsideration and alternatives	17
4.9.1 General	17
4.9.2 Semiconductor microcircuits change	17
4.9.3 Lifetime mitigation solutions	17
4.10 Final report	19
5 Considerations with regard to semiconductor ageing level estimation for semiconductor microcircuits	19
Annex A (informative) Failure and degradation mechanisms of COTS semiconductor microcircuits	20
Annex B (informative) Example of operating and thermal mission profile for a COTS semiconductor microcircuit	22
Annex C (informative) Risk of failure and degradation mechanisms according to the type of COTS semiconductor microcircuit	23

Annex D (informative) BEOL and FEOL technological parameters	24
Annex E (informative) Generic acceleration models	25
Annex F (informative) Final report.....	26
Bibliography.....	28
Figure 1 – Process flow for lifetime assessment and selection of COTS semiconductor microcircuits	11
Figure B.1 – Example of thermal and operating mission profile for a semiconductor microcircuit implemented in an electronic equipment located on the avionic bay of a civil aircraft, assuming 30 °C of thermal dissipation	22
Table A.1 – Some failure and degradation mechanisms for COTS semiconductor microcircuits	20
Table C.1 – Typical failure and degradation mechanisms according to the COTS semiconductor microcircuit family and structure	23
Table D.1 – BEOL and FEOL technological parameters	24
Table E.1 – Examples of generic acceleration model based on the failure and degradation mechanism, and based on the internal semiconductor microcircuit structure	25
Table F.1 – Template for final report.....	26

Sample Document

get full document from standards.iteh.ai

INTERNATIONAL ELECTROTECHNICAL COMMISSION

**Process management for avionics -
Electronic components capability in operation -
Part 2: Semiconductor microcircuit lifetime**

FOREWORD

- 1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
- 2) The formal decisions or agreements of IEC on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested IEC National Committees.
- 3) IEC Publications have the form of recommendations for international use and are accepted by IEC National Committees in that sense. While all reasonable efforts are made to ensure that the technical content of IEC Publications is accurate, IEC cannot be held responsible for the way in which they are used or for any misinterpretation by any end user.
- 4) In order to promote international uniformity, IEC National Committees undertake to apply IEC Publications transparently to the maximum extent possible in their national and regional publications. Any divergence between any IEC Publication and the corresponding national or regional publication shall be clearly indicated in the latter.
- 5) IEC itself does not provide any attestation of conformity. Independent certification bodies provide conformity assessment services and, in some areas, access to IEC marks of conformity. IEC is not responsible for any services carried out by independent certification bodies.
- 6) All users should ensure that they have the latest edition of this publication.
- 7) No liability shall attach to IEC or its directors, employees, servants or agents including individual experts and members of its technical committees and IEC National Committees for any personal injury, property damage or other damage of any nature whatsoever, whether direct or indirect, or for costs (including legal fees) and expenses arising out of the publication, use of, or reliance upon, this IEC Publication or any other IEC Publications.
- 8) Attention is drawn to the Normative references cited in this publication. Use of the referenced publications is indispensable for the correct application of this publication.
- 9) IEC draws attention to the possibility that the implementation of this document may involve the use of (a) patent(s). IEC takes no position concerning the evidence, validity or applicability of any claimed patent rights in respect thereof. As of the date of publication of this document, IEC had not received notice of (a) patent(s), which may be required to implement this document. However, implementers are cautioned that this may not represent the latest information, which may be obtained from the patent database available at <https://patents.iec.ch>. IEC shall not be held responsible for identifying any or all such patent rights.

IEC TR 62240-2, which is a Technical Report, has been prepared by IEC technical committee 107: Process management for avionics. It is a Technical Report.

This second edition cancels and replaces the first edition published in 2018. This edition constitutes a technical revision.

This edition includes the following significant technical changes with respect to the previous edition:

- a) introduction of an additional alternative path and approach where lifetime is assessed by the original component manufacturer based on user or original equipment manufacturer microcircuit mission profile;
- b) update of Figure 1 with regard to the introduction of the additional alternative path & approach;

- c) removal of the mention of SiC & GaN technologies from the considerations in 4.2.2 as the Scope indicates that the principles (process and method) described in this document can be applied to all types of semiconductor technologies.

The text of this Technical Report is based on the following documents:

Draft	Report on voting
107/447/DTR	107/449/RVDTR

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this Technical Report is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/publications.

A list of all parts in the IEC 62240 series, published under the general title *Process management for avionics - Electronic components capability in operation*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under webstore.iec.ch in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn, or
- revised.

INTRODUCTION

Electronic equipment for aerospace, defence and high performance (ADHP) applications integrates more and more commercial off the shelf (COTS) semiconductor microcircuits. These semiconductor microcircuits are above all designed and produced to address high volume and low cost markets such as consumer electronics, telecommunications or microcomputers, whose main requirements are basically cost, integration, performance and low consumption and for which the long term reliability in severe environments (for example vibration, thermal cycling, humidity and operating temperature) is not necessarily an imperative design criterion.

With semiconductor transistor feature size decrease, mainly from 90 nm transistor feature size, wear-out can arise in COTS semiconductor microcircuits. For example, non-homothetic evolution of semiconductor microcircuit bias voltage and transistor feature size scaling have led to an increase of the electrical fields inside the semiconductor microcircuit and hence changes in classical failure and degradation modes or mechanisms. In addition new transistor architectures and technologies (for example fin field effect transistor (FinFET), fully depleted silicon on insulator (FD-SOI), etc.) and new materials (for example low-k dielectrics, high-k dielectrics, strain source/drain Si-Ge) have been introduced since the generation 90 nm, and particularly from 45 nm and below, to overcome the scaling issues, contributing potentially to the evolution of failure and degradation modes or mechanisms.

In this context, it might not be possible for the lifetime of new generations of COTS semiconductor microcircuits to meet the lifetime requirements of high performance, high reliability and long duration electronic applications (for example twenty years, thirty years or more). As a consequence, specific reliability assessment and maintenance plans are considered within the semiconductor microcircuit selection activities.

Sample Document

get full document from standards.iteh.ai

1 Scope

This part of IEC 62240, which is a Technical Report, focuses on original equipment manufacturers (OEMs) using commercial off the shelf (COTS) semiconductor microcircuits for high performance, high reliability and long duration applications. This document supports OEMs in the preparation and maintenance of their semiconductor electronic component management plan (ECMP).

NOTE 1 OEMs are responsible for applications reliability performance that semiconductor microcircuit lifetime can affect; They are thus responsible for the compliance of the lifetime of the semiconductor microcircuits they use with the lifetime requirements of the microcircuits under the applications mission conditions.

This document describes a process and a method for selecting digital semiconductor microcircuits by ensuring that their lifetime is compatible with the requirements of aerospace, defence and high performance (ADHP) applications (generally in connection with functional environments). Methods and guidelines are provided to assess the long-term reliability of COTS semiconductor microcircuits in such applications; they mainly apply during the electronic design phase when selecting semiconductor microcircuits and assessing the application reliability.

Moreover, this document focuses on the intrinsic wear-out and the lifetime of COTS semiconductor microcircuits processed of less than or equal to 90 nm feature size (also called deep sub-micron (DSM) semiconductor microcircuits) and puts aside, at this time, packaging wear-out and random failure mechanisms. In this view, physics of failure (PoF) is at the heart of the approach.

Indeed 90 nm process node was a bend for realizing that the semiconductor wear-out and lifetime was a concern for microcircuits processed with nodes from 90 nm and below with regard to aerospace, defence and high performance (ADHP) mission profile.

Particularly from 45 nm and below, wear-out and lifetime remains a serious concern for long term ADHP missions. In addition, from 28 nm, scaling is no longer a classical technology shrink (case of planar technology for example) and different technological architectures of transistors are introduced (for example: fin field-effect transistors (FinFETs), gate-all-around field-effect transistors (GAAFETs)); semiconductor microcircuits in such technologies are often named ultra-deep sub-micron (UDSM).

Although developed for COTS deep sub-micron (DSM) semiconductor microcircuits based on silicon, the high-level approach and principles (process and method) described in this document can apply to all types of devices technologies, for example devices processed with a gallium nitride (GaN) technology or a silicon carbide (SiC) technology.

NOTE 2 IEC 62239-1 can assist OEMs in the creation and maintenance of ECMPs.

NOTE 3 SAE ARP6338 can also help the OEM with regard to assessment and mitigation of wear-out of life-limited semiconductor microcircuits.

NOTE 4 With the evolution of electronic technology and semiconductor microcircuits processed of less than or equal to 90 nm feature size, the current MIL-HDBK-217 handbook or FIDES guide become inappropriate as they are based for the time being on the assumption that the semiconductor electronic component exhibits a constant (random) failure rate and does not have life limits or exhibit wear-out.

Moreover, silicon itself has fundamentally very low failures in time (FIT) rates and the major failure modes are often in the packaging (for example housing, bond wires, etc.).

Although developed for the avionics industry, this process can be applied by other industrial sectors.

2 Normative references

There are no normative references in this document.

3 Terms, definitions and abbreviated terms

3.1 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminology databases for use in standardization at the following addresses:

- IEC Electropedia: available at <https://www.electropedia.org/>
- ISO Online browsing platform: available at <https://www.iso.org/obp>

3.1.1

acceleration model

equation for predicting time-to-fail as a function of operating stress

Note 1 to entry: An acceleration model shows how time-to-fail at a particular operating stress level can be used to predict the equivalent time-to-fail at a different operating stress level.

Note 2 to entry: An acceleration model is associated to one failure and degradation mode or mechanism. Acceleration models can be either defined for temperature, electrical, mechanical, environmental, or other stresses that can affect the reliability of a device.

Note 3 to entry: An acceleration model is semi-empirical and is basically based on the physics of failure. Times are generally derived from modeled time-to-failure distributions (lognormal, Weibull, exponential, etc.).

Note 4 to entry: The acceleration model is also defined as acceleration factor, for which the abbreviated term AF is used.

3.1.2

cold redundancy

technique where one primary part is operational and the redundant one is in a backup mode

Note 1 to entry: The redundant part can also be called "cold" part and generally it is technically identical to the primary part.

Note 2 to entry: The "cold" part can be non-powered or in a standby mode and it is usually called upon only on failure of the primary part.

3.1.3

electronic equipment

functioning electronic device produced by the plan owner, which incorporates electronic components

Note 1 to entry: End items, sub-assemblies, line-replaceable units and shop-replaceable units are examples of electronic equipment.

[SOURCE: IEC 62239-1:2018, 3.1.20]

3.1.4

high-k dielectrics

material with a high dielectric constant "k" (as compared to silicon dioxide)

Note 1 to entry: High-k dielectrics are used in semiconductor manufacturing processes where they are usually used to replace a silicon dioxide gate dielectric or another dielectric layer of a semiconductor microcircuit. The implementation of high-k gate dielectrics is one of several strategies developed to allow continued scaling and miniaturization of semiconductor microcircuits.

3.1.5

lifetime

upper bound of period of time during which the COTS semiconductor component performs a required function without failure under stated conditions