

TECHNICAL REPORT

REDLINE VERSION

**Process management for avionics - Electronic components capability in
operation -
Part 2: Semiconductor microcircuit lifetime**

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

**Process management for avionics -
Electronic components capability in operation -
Part 2: Semiconductor microcircuit lifetime**

FOREWORD

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IEC TR 62240-2, which is a Technical Report, has been prepared by IEC technical committee 107: Process management for avionics. It is a Technical Report.

This second edition cancels and replaces the first edition published in 2018. This edition constitutes a technical revision.

This edition includes the following significant technical changes with respect to the previous edition:

- a) introduction of an additional alternative path and approach where lifetime is assessed by the original component manufacturer based on user or original equipment manufacturer microcircuit mission profile;
- b) update of Figure 1 with regard to the introduction of the additional alternative path & approach;
- c) removal of the mention of SiC & GaN technologies from the considerations in 4.2.2 as the Scope indicates that the principles (process and method) described in this document can be applied to all types of semiconductor technologies.

The text of this Technical Report is based on the following documents:

Draft	Report on voting
107/447/DTR	107/449/RVDTR

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this Technical Report is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/publications.

A list of all parts in the IEC 62240 series, published under the general title *Process management for avionics - Electronic components capability in operation*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under webstore.iec.ch in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn, or
- revised.

INTRODUCTION

Electronic equipment for aerospace, defence and high performance (ADHP) applications integrates more and more commercial off the shelf (COTS) semiconductor microcircuits. These semiconductor microcircuits are above all designed and produced to address high volume and low cost markets such as consumer electronics, telecommunications or microcomputers, whose main requirements are basically cost, integration, performance and low consumption and for which the long term reliability in severe environments (for example vibration, thermal cycling, humidity and operating temperature) is not necessarily an imperative design criterion.

With semiconductor transistor feature size decrease, mainly from 90 nm transistor feature size, wear-out can arise in COTS semiconductor microcircuits. For example, non-homothetic evolution of semiconductor microcircuit bias voltage and transistor feature size scaling have led to an increase of the electrical fields inside the semiconductor microcircuit and hence changes in classical failure and degradation modes or mechanisms. In addition new transistor architectures and technologies (for example fin field effect transistor (FinFET), fully depleted silicon on insulator (FD-SOI), etc.) and new materials (for example low-k dielectrics, high-k dielectrics, strain source/drain Si-Ge) have been introduced since the generation 90 nm, and particularly from 45 nm and below, to overcome the scaling issues, contributing potentially to the evolution of failure and degradation modes or mechanisms.

In this context, it might not be possible for the lifetime of new generations of COTS semiconductor microcircuits ~~may not~~ to meet the lifetime requirements of high performance, high reliability and long duration electronic applications (for example twenty years, thirty years or more). As a consequence, specific reliability assessment and maintenance plans are considered within the semiconductor microcircuit selection activities.

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1 Scope

This part of IEC 62240, which is a Technical Report, focuses on original equipment manufacturers (OEMs) using commercial off the shelf (COTS) semiconductor microcircuits for high performance, high reliability and long duration applications. This document supports OEMs in the preparation and maintenance of their semiconductor electronic component management plan (ECMP).

NOTE 1 OEMs are responsible for applications reliability performance that semiconductor microcircuit lifetime can affect; They are thus responsible for the compliance of the lifetime of the semiconductor microcircuits they use with the lifetime requirements of the microcircuits under the applications mission conditions.

This document describes a process and a method for selecting digital semiconductor microcircuits by ensuring that their lifetime is compatible with the requirements of aerospace, defence and high performance (ADHP) applications (generally in connection with functional environments). Methods and guidelines are provided to assess the long-term reliability of COTS semiconductor microcircuits in such applications; they mainly apply during the electronic design phase when selecting semiconductor microcircuits and assessing the application reliability.

Moreover, this document focuses on the intrinsic wear-out and the lifetime of COTS semiconductor microcircuits processed of less than or equal to 90 nm feature size (also called deep sub-micron (DSM) semiconductor microcircuits) and puts aside, at this time, packaging wear-out and random failure mechanisms. In this view, physics of failure (PoF) is at the heart of the approach.

Indeed 90 nm process node was a bend for realizing that the semiconductor wear-out and lifetime was a concern for microcircuits processed with nodes from 90 nm and below with regard to aerospace, defence and high performance (ADHP) mission profile.

Particularly from 45 nm and below, wear-out and lifetime remains a serious concern for long term ADHP missions. In addition, from 28 nm, scaling is no longer a classical technology shrink (case of planar technology for example) and different technological architectures of transistors are introduced (for example: fin field-effect transistors (FinFETs), gate-all-around field-effect transistors (GAAFETs)); semiconductor microcircuits in such technologies are often named ultra-deep sub-micron (UDSM).

Although developed for COTS deep sub-micron (DSM) semiconductor microcircuits based on silicon, the high-level approach and principles (process and method) described in this document can apply to all types of devices technologies, for example devices processed with a gallium nitride (GaN) technology or a silicon carbide (SiC) technology.

NOTE 2 IEC 62239-1 can assist OEMs in the creation and maintenance of ECMPs.

NOTE 3 SAE ARP6338 can also help the OEM with regard to assessment and mitigation of wear-out of life-limited semiconductor microcircuits.

NOTE 4 With the evolution of electronic technology and semiconductor microcircuits processed of less than or equal to 90 nm feature size, the current MIL-HDBK-217 handbook or FIDES guide become inappropriate as they are based for the time being on the assumption that the semiconductor electronic component exhibits a constant (random) failure rate and does not have life limits or exhibit wear-out.

Moreover, silicon itself has fundamentally very low failures in time (FIT) rates and the major failure modes are often in the packaging (for example housing, bond wires, etc.).

Although developed for the avionics industry, this process can be applied by other industrial sectors.

2 Normative references

There are no normative references in this document.

3 Terms, definitions and abbreviated terms

3.1 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminology databases for use in standardization at the following addresses:

- IEC Electropedia: available at <https://www.electropedia.org/>
- ISO Online browsing platform: available at <https://www.iso.org/obp>

3.1.1

acceleration model

equation for predicting time-to-fail as a function of operating stress

Note 1 to entry: An acceleration model shows how time-to-fail at a particular operating stress level can be used to predict the equivalent time-to-fail at a different operating stress level.

Note 2 to entry: An acceleration model is associated to one failure and degradation mode or mechanism. Acceleration models can be either defined for temperature, electrical, mechanical, environmental, or other stresses that can affect the reliability of a device.

Note 3 to entry: An acceleration model is semi-empirical and is basically based on the physics of failure. Times are generally derived from modeled time-to-failure distributions (lognormal, Weibull, exponential, etc.).

Note 4 to entry: The acceleration model is also defined as acceleration factor, for which the abbreviated term AF is used.

3.1.2

Bi-CMOS bipolar CMOS

~~technology integrating two separate semiconductor technologies, bipolar junction transistor and CMOS transistor, in a single electronic component~~

3.1.2

cold redundancy

technique where one primary part is operational and the redundant one is in a backup mode

Note 1 to entry: The redundant part can also be called "cold" part and generally it is technically identical to the primary part.

Note 2 to entry: The "cold" part can be non-powered or in a standby mode and it is usually called upon only on failure of the primary part.

3.1.3

electronic equipment

functioning electronic device produced by the plan owner, which incorporates electronic components

Note 1 to entry: End items, sub-assemblies, line-replaceable units and shop-replaceable units are examples of electronic equipment.

[SOURCE: IEC 62239-1:2018, 3.1.20]

3.1.4

high-k dielectrics

material with a high dielectric constant "k" (as compared to silicon dioxide)

Note 1 to entry: High-k dielectrics are used in semiconductor manufacturing processes where they are usually used to replace a silicon dioxide gate dielectric or another dielectric layer of a semiconductor microcircuit. The implementation of high-k gate dielectrics is one of several strategies developed to allow continued scaling and miniaturization of semiconductor microcircuits.

3.1.5**lifetime**

upper bound of period of time during which the COTS semiconductor component performs a required function without failure under stated conditions

3.1.6**low-k dielectrics**

material with a small dielectric constant "k", relative to silicon dioxide

Note 1 to entry: Low-k dielectric material implementation is one of several strategies used to allow continued scaling and miniaturization of semiconductor microcircuits.

3.1.7**NAND****Negative-AND**

logic gate which produces, in digital electronics, an output that is false (0) only if all its inputs are true (1) and an output true (1) if one or both inputs are false (0)

[SOURCE: IEC 62239-1:2018, 3.1.22]

3.1.8**NOR****Negative-OR**

logic gate which produces, in digital electronics, an output that is true (1) if both the inputs are false (0) and an output false (0) if one or both inputs are true (1)

[SOURCE: IEC 62239-1:2018, 3.1.23]

3.1.9**plan owner**

original design authority responsible for all aspects of the design, functionality and reliability of the delivered equipment in the intended application and responsible for writing and maintaining their specific ECMP

[SOURCE: IEC 62239-1:2018, 3.1.26]

3.1.10**process node**

specific semiconductor manufacturing process and its design geometry rules

Note 1 to entry: Generally, a smaller technology node means a smaller feature size, producing smaller transistors which are both faster and more power-efficient. Historically, the name "process node" referred to a number of different features of a transistor including the gate length as well as the first layer metal half-pitch. Most recently, due to various marketing practices and discrepancies among foundries, the name "process node" has lost the exact meaning it once held. Recent technology nodes below 90 nm refer purely to a specific generation of semiconductor microcircuits made in a particular technology; they do not correspond to any gate length or half pitch. Nevertheless the name convention has stuck and it is what the leading foundries call their nodes.

Note 2 to entry: Process node is also called technology node or simply node.

3.1.11**semiconductor microcircuit****semiconductor electronic component**

electrical or electronic device that is not subject to disassembly without destruction or impairment of design use and that utilises the properties of semiconductor materials

Note 1 to entry: It is sometimes called electronic part or electronic piece part or electronic device or electronic component or integrated circuits. It refers to active electronic parts such as memories, microcontrollers, microprocessors, etc.

3.1.12**wear-out**

phenomenon resulting in a permanent physical degradation of a semiconductor that can be quantified through a quasi-deterministic lifetime indicator

3.2 Abbreviated terms

ADHP	aerospace, defence and high performance
AF	acceleration factor
BEOL	back end of the line
BTI	bias temperature instability
COTS	commercial off the shelf (related to semiconductor microcircuits for the purposes of this document)
CMOS	complementary metal-oxide semiconductor
DDR	double data rate (memory)
DPA	deprocessing analysis
DRAM	dynamic random access memory
DSM	deep sub-micron
ECMP	electronic component management plan
EM	electro-migration
EOT	equivalent oxide thickness
FD-SOI	fully depleted silicon on insulator
FEOL	front end of the line
FeRAM	ferroelectric random access memory
FinFET	fin field effect transistor
FIT	failures in time (number of failures that can be expected in one billion device-hours of operation)
FPGA	field programmable gate array
GAAFET	gate-all-around field-effect transistors
GaN	gallium nitride
Ge	germanium
HCI	hot carrier injection
I/O	input/output
MOSFET	metal-oxide-semiconductor field-effect transistor
MRAM	magnetic random access memory
NMOS	N metal-oxide semiconductor
OCM	original component manufacturer (related to the COTS electronic components manufacturer)
OEM	original equipment manufacturer
PMOS	P metal-oxide semiconductor
PoF	physics of failure
ReRAM	resistive random access memory
Si	silicon
SiC	silicon carbide
SDRAM	synchronous dynamic random access memory
SRAM	static random access memory
TDDB	time dependent dielectric breakdown
TTF _x %	time to failure (or lifetime) for x % of samples
UDSM	ultra-deep sub-micron

4 Lifetime assessment process and method

4.1 General

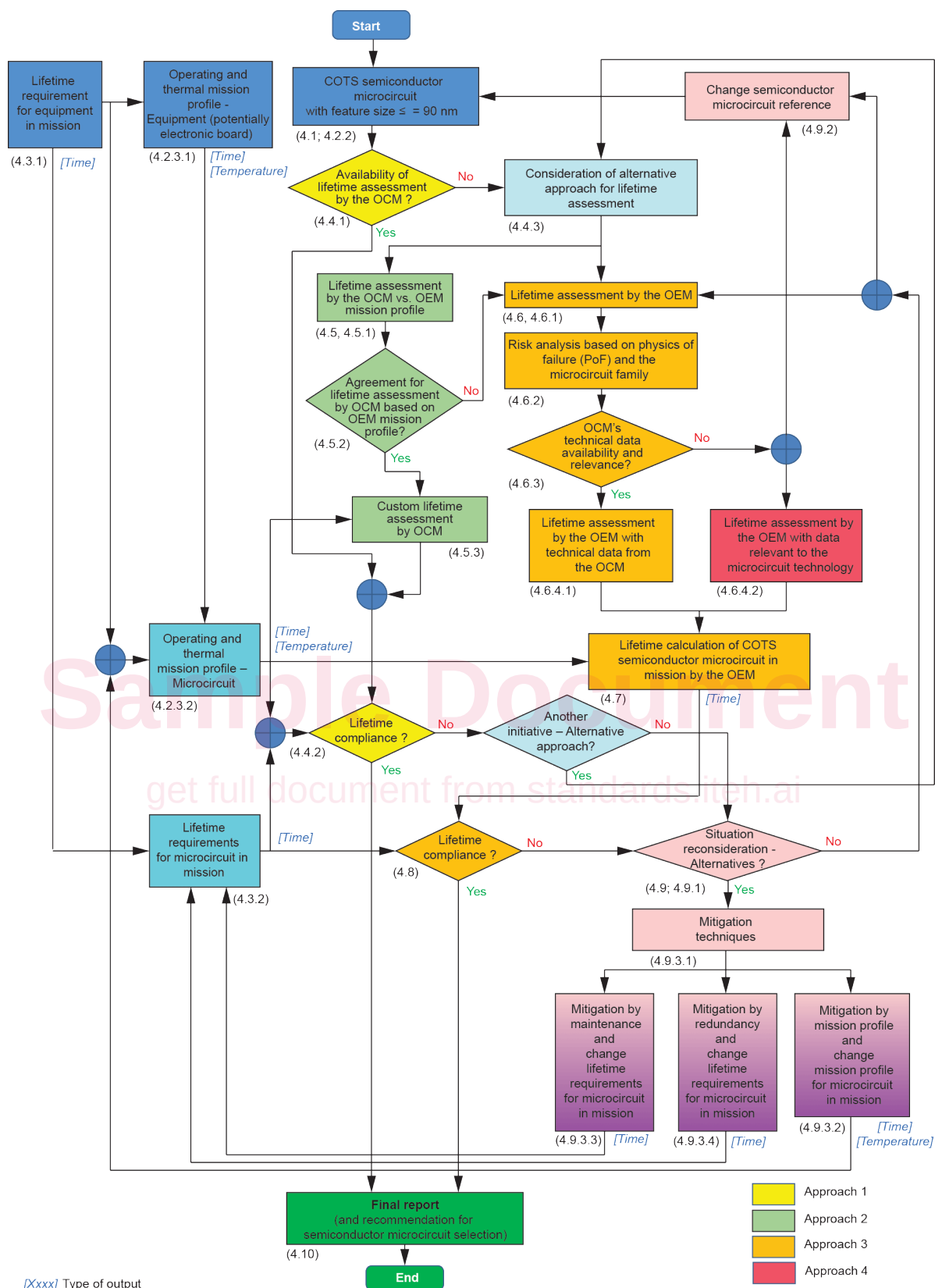
The aim of the method is twofold. In a first step, this method allows the assessment and determination of the lifetime of a COTS semiconductor microcircuit in a specific environment, and in the second step it provides the means for the OEM to select the right COTS semiconductor microcircuit according to the electronic equipment reliability requirements.

The method is synthesized in the process flow of Figure 1.

Moreover, according to the level of information available from the OCMs or silicon foundries, or both, ~~three~~ four different paths can be considered:

- path and approach 1 (represented in yellow in Figure 1) where the OEM considers for its application the lifetime assessment of the COTS semiconductor microcircuit with regard to the lifetime specified and associated technical data provided by the OCM;
- path and approach 2 (represented in light green in Figure 1) where the lifetime is assessed by the OCM according to the COTS semiconductor microcircuit mission profile of the OEM; this approach requires a close collaboration between the OCM and the OEM;
- path and approach ~~2~~3 (represented in orange in Figure 1) where, in the absence of lifetime data specified by the OCM or if associated technical data are incomplete, the OEM conducts for its application its own lifetime assessment of the COTS semiconductor microcircuit, making a risk analysis and using the available technical data (for example, failure and degradation mechanisms, acceleration models, raw qualification test results) provided by the OCM;
- path and approach ~~3~~4 (represented in burgundy in Figure 1) where, in case of unavailability or irrelevancy of OCM technical data, the OEM conducts for its application its own lifetime assessment of the COTS semiconductor microcircuit collecting potential technical data and considering the technology of the semiconductor microcircuit (including potential deprocessing analysis (DPA)).





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Figure 1 – Process flow for lifetime assessment and selection of COTS semiconductor microcircuits

4.2 Input data for the method

4.2.1 General

The input data for the method are as follows.

4.2.2 COTS semiconductor microcircuits and lifetime issues considerations

Wear-out effects are mainly driven by the electrical fields induced by the electrical bias of the FEOL and BEOL stack of the semiconductor and by the increased current density with regard to electromigration in particular. In this view, technologies nodes from 5 µm and down to the 0,1 µm were designed by the OCM to ensure constant electrical fields over the different process node integrations. This was achieved by reducing the core bias voltages and the characteristic dimension of the transistors with a same integration factor (around 0,3). However below 0,1 µm, this homothetic scaling of the bias core and I/O voltages was no longer possible. Therefore, the electrical fields become more important, and the wear-out effects start to increase compared to previous generation nodes.

NOTE Linked with scaling and semiconductor transistor feature size decrease, technological improvements on barrier metals and alloys are regularly proposed in order to cope with the increased current density that conductors have to carry. As the current density is the major factor that impacts electromigration, it is important to consider the scaling effects on electromigration reliability (for more information see [5] and [17]¹).

Lifetime assessment is performed on microcircuits processed with nodes from 90 nm and below with regard to requirement and ADHP mission profile, and in particular with regard to some long term ADHP mission profile severity (equipment mission profile with, for example, quasi continuous operation and highly severe and very many equipment thermal cycles, etc.).

It is particularly important to consider and assess wear-out effects and lifetime ~~considerations need to be taken into account~~ for electronic designs using COTS semiconductor microcircuits manufactured in ~~90 45 nm~~ process nodes and below. ~~This includes digital COTS semiconductor microcircuits such as SRAM, DRAM (SDRAM, DDR series), flash memories (NOR logic gate, NAND logic gate), MRAM, microcontrollers, microprocessors and FPGA. Analog or Bi-CMOS electronic components can also be concerned and a similar approach can be used.~~

This includes:

- CMOS microcircuits: micro processors, microcontrollers, FPGA, SRAM;
- memories: DRAM (SDRAM, DDR series), flash memories (NAND logic gate, NOR logic gate), MRAM, FeRAM, ReRAM.

The process node can be obtained from the original component manufacturer's datasheet ~~or indicated on the part number marking~~ or by contacting the OCM directly.

Intrinsic failures and degradations of semiconductor microcircuits which can impact wear-out are typically electro-migration (EM), time-dependent dielectric breakdown (TDDB), hot carrier injection (HCI), and bias temperature instability (BTI). Annex A provides more details.

4.2.3 Operating and thermal conditions

4.2.3.1 Operating and thermal mission profiles of the electronic equipment

The OEM usually obtains this information through the electronic equipment specification, standards, or customer requirements.

¹ Numbers in square brackets refer to the Bibliography.