SLOVENSKI STANDARD
oSIST prEN IEC 60749-29:2026

01-marec-2026

Polprevodniški elementi - Mehanske in klimatske preskusne metode - 29. del: Preskus zapore

Semiconductor devices - Mechanical and climatic test methods - Part 29: Latch-up test

Halbleiterbauelemente - Mechanische und klimatische Prüfverfahren - Teil 29: Latch-up-Prüfung

iTeh Standards
(https://standards.iteh.ai)
Document Preview

Dispositifs à semiconducteurs - Méthodes d'essai mécaniques et climatiques - Partie 29: Essai de verrouillage

Ta slovenski standard je istoveten z: **prEN IEC 60749-29:2026**

---

oSIST prEN IEC 60749-29:2026
https://standards.iteh.ai/catalog/standards/sist/a9aebe99-6196-479c-833e-393a4ffb125b/osist-pren-iec-60749-29-2026

ICS:

19.020	Preskuševalni pogoji in postopki na splošno	Test conditions and procedures in general
31.080.01	Polprevodniški elementi (naprave) na splošno	Semiconductor devices in general

oSIST prEN IEC 60749-29:2026 **en**

2003-01.Slovenski inštitut za standardizacijo. Razmnoževanje celote ali delov tega standarda ni dovoljeno.

iTeh Standards
(https://standards.iteh.ai)
Document Preview

oSIST prEN IEC 60749-29:2026
https://standards.iteh.ai/catalog/standards/sist/a9aebe99-6196-479c-833e-393a4ffb125b/osist-pren-iec-60749-29-2026

47/2991/CDV

COMMITTEE DRAFT FOR VOTE (CDV)

PROJECT NUMBER: **IEC 60749-29 ED3**	
DATE OF CIRCULATION: **2026-01-30**	CLOSING DATE FOR VOTING: **2026-04-24**
SUPERSEDES DOCUMENTS: **47/2971/RR**	

IEC TC 47 : SEMICONDUCTOR DEVICES	
SECRETARIAT: Korea, Republic of	SECRETARY: Mr Cheolung Cha
OF INTEREST TO THE FOLLOWING COMMITTEES:	HORIZONTAL FUNCTION(S):
ASPECTS CONCERNED: Environment	
☒ SUBMITTED FOR CENELEC PARALLEL VOTING **Attention IEC-CENELEC parallel voting** The attention of IEC National Committees, members of CENELEC, is drawn to the fact that this Committee Draft for Vote (CDV) is submitted for parallel voting. The CENELEC members are invited to vote through the CENELEC online voting system.	☐ NOT SUBMITTED FOR CENELEC PARALLEL VOTING

iTeh Standards
(https://standards.iteh.ai)
Document Preview
oSIST prEN IEC 60749-29:2026
https://standards.iteh.ai/catalog/standards/sist/a9aebe99-6196-479c-833e-393a4ffb125b/osist-pren-iec-60749-29-2026

This document is still under study and subject to change. It should not be used for reference purposes.

Recipients of this document are invited to submit, with their comments, notification of any relevant patent rights of which they are aware and to provide supporting documentation.

Recipients of this document are invited to submit, with their comments, notification of any relevant "In Some Countries" clauses to be included should this proposal proceed. Recipients are reminded that the CDV stage is the final stage for submitting ISC clauses. (SEE AC/22/2007 OR NEW GUIDANCE DOC).

TITLE:

Semiconductor devices - Mechanical and climatic test methods - Part 29: Latch-up test

PROPOSED STABILITY DATE: 2031

NOTE FROM TC/SC OFFICERS:

Copyright © 2025 International Electrotechnical Commission, IEC. All rights reserved. It is permitted to download this electronic file, to make a copy and to print out the content for the sole purpose of preparing National Committee positions. You may not copy or "mirror" the file or printed version of the document, or any part of it, for any other purpose without permission in writing from IEC.

CONTENTS

Foreword 3
1 Scope 8
2 Normative references 8
3 Terms and definitions 9
4 Latch-up characterization 14
  4.1 General description 14
  4.2 Latch-up immunity 14
  4.3 Temperature Classification 15
  4.4 Overall requirement classifications 15
5 Apparatus and material 15
  5.1 Latch-up tester 15
    5.1.1 Hardware Requirements and Capabilities 15
    5.1.2 Test Board 16
    5.1.3 Temperature Control 16
6 Latch-up test procedure 17
  6.1 General Latch-Up Test Overview 17
  6.2 Device Handling 19
  6.3 Sample Size 19
  6.4 Preparation of the Latch-Up Test 19
    6.4.1 Pin Types and Grouping 19
    6.4.2 Power Supply Assignments 20
    6.4.3 Product Pre-Conditioning 21
    6.4.4 Device Temperature Set-Up 21
  6.5 Latch-Up Detection Criteria 21
    6.5.1 Latch-Up Detection 21
    6.5.2 Power Supply Current Limits 22
  6.6 Signal Pin Test 23
    6.6.1 Signal Pin Test Flow 23
    6.6.2 Waveforms for the Positive Signal Pin Tests 25
    6.6.3 Waveforms for the negative signal pin test – I Test / E Test 28
  6.7 Supply Test 31
    6.7.1 Supply Test Flow 31
    6.7.2 Waveforms for the Supply Test 33
  6.8 Functional and parametric test after latch-up stress 34
  6.9 Failure analysis 34
  6.10 DUR disposition 35
7 Report requirements 35
  7.1 Report normatives 35
Annex A (informative) Special pins 36
  A.1 Purpose 36
  A.2 Pins creating latch-up challenges 36
  A.3 Definition of special pins 37
  A.4 Special pin guidance 37
Annex B (informative) Calculations for junction, ambient or case temperature 48

iTeh Standards
(https://standards.iteh.ai)
Document Preview
oSIST prEN IEC 60749-29:2026
https://standards.iteh.ai/catalog/standards/sist/a9acbe99-6196-479c-833e-393a4ff0125b/osist-pren-iec-60749-29-2026

B.1 Calculating operating ambient temperature T_a or T_j from one known temperature 48
B.2 Calculating operating case temperature T_c or T_j from one known temperature 49
B.3 Temperature monitoring and control equipment 49
B.4 Device temperature control 50
B.4.1 Temperature control methodology 50
B.4.2 Class II testing 50
B.4.3 T_{jmax} determination 51
Annex C (informative) Equivalent circuits for latch-up testing 52
Annex D (informative) Reporting data examples 56
Annex E (informative) Determining MSV 57
Annex F (Informative) Pulse Source Verification 62
F.1 Introduction 62
F.2 Verification test setup 62
F.3 Standard pulse 63
F.4 I-Test 63
F.5 E-Test and supply test 65
F.6 Specialized pulse source verification 67
F.7 Sample pulse measurements 67
Annex G (Informative) Signal pin test – I-Test vs E-Test – How to decide which is best 70
Annex H (Informative) Controlling pin under test during pre- and post-stress 71

Figure 1 – General Latch-Up Test Flow for the Signal Pin Test and Supply Tests. 18
Figure 2 – Signal pin test flow example: positive current stress with input pins biased to low (V_{minOP}). Also applicable to V_{maxOP} 24
Figure 1 – Test waveform for positive signal pin test (I Test) 26
Figure 5 – Test waveform for negative signal pin test (I Test) 29
Figure 6 – Test waveform for negative signal pin test (E Test) 30
Figure 7 – Supply test flow example: power supply stress with input pins biased to low (V_{minOP}) and to high (V_{maxOP}) 32
Figure 8 — Test waveform for the supply test 33
Figure 9 – Pins connected through passive components 38
Figure 10 – Differential Inputs: Op Amp inputs, clock oscillators, comparators 39
Figure 11 – Inputs, Outputs, IOs powered by internal power domain 39
Figure 12 – Input / Output Pair with an Inverter in-between 39
Figure 13 – Pins with digital and/or analog circuits multiplexed 40
Figure 14 – RF pins with direct connection to ground 40
Figure 15 – Temperature sensing diode pins 40
Figure 17 – Voltage and current reference pins 41
Figure 18 – Voltage monitor and sense pins 41
Figure 19 – Current sense pins 41
Figure 20 – DC voltage regulators 42
Figure 21 – Switched voltage regulators 43
Figure 22 – Circuits with multiple supply sources 43
Figure 23 – Non-volatile programming pins 44

iTeh Standards
(https://standards.iteh.ai)
Document Preview
oSIST prEN IEC 60749-29:2026
https://standards.iteh.ai/catalog/standards/sist/a9aebe99-6196-479c-833e-393a4ffb125b/osist-pren-iec-60749-29-2026

oSIST prEN IEC 60749-29:2026

Figure 24 – Power supplies with specific relationships 44
Figure 25 – Example 1: Complex microcontroller 44
Figure 26 – Example 1: as used in a typical application 45
Figure 27 – Example 2: Differential comparator 45
Figure 28 – Example 3: Non-integrated regulator 46
Figure 29 – Example 4: Integrated regulator 47
Figure 30 – Equivalent circuit for positive current pulse signal pin test latch-up testing 52
Figure 31 – Equivalent circuit for positive voltage pulse signal pin test latch-up testing........53
Figure 32 – Equivalent circuit for negative current pulse signal pin test latch-up testing 54
Figure 33 – Equivalent circuit for negative voltage pulse signal pin test latch-up testing 54
Figure 34 — Equivalent circuit for supply test latch-up testing 55
Figure 35 – Electrical stress chart for latch-up stress and MSV 58
Figure 36 --- Verification test set-up 63
Figure 37 – Comparison of 2 pulses intended to create a 100 mA pulse Through a 20 Ohm resistor 68
Figure 38 – Comparison of 3 pulses intended to create a 100 mA pulse through a 1 kΩ resistor 69
Figure 39 – Pre-stress and post-stress current and voltage control 71

Table 1 – Latch-up immunity levels 14
Table 2 – Overview of latch-up tests for a complete latch-up characterization 19
Table 3 – Latch-Up Detection Criteria 21
Table 4 – Pulse current and voltage requirements for the positive signal pin test 27
Table 5 – Timing Requirements for the Signal Pin Test and the Supply Test 28
Table 6 – Pulse current and voltage requirements for the negative signal pin test 30
Table 7 – Pulse current and voltage requirements for the supply test 34
Table 8 – DC regulator cross references 41
Table 9 – Samples of verification resistor values for positive I Test pulse verification for different technologies being tested 64
Table 10 – Samples of verification resistor values for negative I Test pulse verification for different technologies being tested 65
Table 11 – Samples of verification resistor values for positive E Test pulse verification for different technologies being tested 66
Table 12 – Samples of verification resistor values for negative E Test pulse verification for different technologies being tested 66
Table 15 – Example 1(b) Pre-stress conditions 72
Table 16 – Example 1(b) Post-stress conditions 72
Table 17 – Example 2 Pre-stress conditions 73
Table 18 – Example 2 Pre-stress conditions 73

iTeh Standards
(https://standards.iteh.ai)
Document Preview
oSIST prEN IEC 60749-29:2026
https://standards.iteh.ai/catalog/standards/sist/a9aebe99-6196-479c-833e-393a4f1b125b/osist-pren-iec-60749-29-2026

INTERNATIONAL ELECTROTECHNICAL COMMISSION

SEMICONDUCTOR DEVICES – MECHANICAL AND CLIMATIC TEST METHODS –

Part 29: Latch-up test

FOREWORD

1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as “IEC Publication(s)”). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
2) The formal decisions or agreements of IEC on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested IEC National Committees.
3) IEC Publications have the form of recommendations for international use and are accepted by IEC National Committees in that sense. While all reasonable efforts are made to ensure that the technical content of IEC Publications is accurate, IEC cannot be held responsible for the way in which they are used or for any misinterpretation by any end user.
4) In order to promote international uniformity, IEC National Committees undertake to apply IEC Publications transparently to the maximum extent possible in their national and regional publications. Any divergence between any IEC Publication and the corresponding national or regional publication shall be clearly indicated in the latter.
5) IEC itself does not provide any attestation of conformity. Independent certification bodies provide conformity assessment services and, in some areas, access to IEC marks of conformity. IEC is not responsible for any services carried out by independent certification bodies.
6) All users should ensure that they have the latest edition of this publication.
7) No liability shall attach to IEC or its directors, employees, servants or agents including individual experts and members of its technical committees and IEC National Committees for any personal injury, property damage or other damage of any nature whatsoever, whether direct or indirect, or for costs (including legal fees) and expenses arising out of the publication, use of, or reliance upon, this IEC Publication or any other IEC Publications.
8) Attention is drawn to the Normative references cited in this publication. Use of the referenced publications is indispensable for the correct application of this publication.
9) Attention is drawn to the possibility that some of the elements of this IEC Publication may be the subject of patent rights. IEC shall not be held responsible for identifying any or all such patent rights.

iTeh Standards
(https://standards.iteh.ai)
Document Preview
oSIST prEN IEC 60749-29:2026
https://standards.iteh.ai/catalog/standards/sist/a9ae8e99-0196-479e-833e-593a4ffb125b/osist-pren-iec-60749-29-2026

International Standard IEC 60749-29 has been prepared by IEC technical committee 47: Semiconductor devices.

This fourth edition cancels and replaces the third edition published in 2010. This edition constitutes a full technical revision. This standard is based upon JEDEC JESD78F.02. It is used with permission of the copyright holder, JEDEC Solid state Technology Association.

The significant changes with respect to the previous edition include:

a) Extensive technical changes to definitions, test methods and classifications;
b) Fully revised annexes covering the testing of pins, voltage domain descriptions and statistics of testing coverage.