
Smernice za postopke vrednotenja zanesljivosti in robustnosti oksida vrat močnostnih silicijevokarbidnih tranzistorjev MOSFET (SiC) (Fast Track, hitri postopek)

Guideline for gate oxide reliability and robustness evaluation procedures for silicon carbide power mosfets (Fast Track)

Sample Document

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TITLE:

Guideline for Gate Oxide Reliability and Robustness Evaluation Procedures for Silicon Carbide Power MOSFETs (Fast Track)

PROPOSED STABILITY DATE: 2030

NOTE FROM TC/SC OFFICERS:

This CDV is based upon JEDEC document JEP194 (title: GUIDELINE FOR GATE OXIDE RELIABILITY AND ROBUSTNESS EVALUATION PROCEDURES FOR SILICON CARBIDE POWER MOSFETs) and is circulated according to the IEC fast-track procedure (see F.2 of ISO/IEC Directives, Part 1). This document is proposed by the US National Committee and WG 8 at its November 2025 meeting approved fast-track procedure and was presented to TC 47 November 2025 Plenary meeting.

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

**GUIDELINE FOR GATE OXIDE RELIABILITY AND ROBUSTNESS EVALUATION
PROCEDURES FOR SILICON CARBIDE POWER MOSFETS**

FOREWORD

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The text of this International Standard is based on the following documents:

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Full information on the voting for the approval of this International Standard can be found in the report on voting indicated in the above table.

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- replaced by a revised edition, or
- amended.

The National Committees are requested to note that for this document the stability date is 20XX.

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INTRODUCTION

(From JEDEC Board Ballot JCB-22-61, formulated under the cognizance of the JC-70.2 Subcommittee on SiC Power Electronic Conversion Semiconductor Standards.)

This document was formulated by JEDEC JC-70.2 SiC Power Electronics Conversion Semiconductor Standards subcommittee consisting of worldwide industry experts from various power semiconductor, power supply and test equipment manufacturing companies.

This document has the purpose of laying out generally acceptable practices for testing gate oxide reliability of silicon carbide (SiC) based power devices having a gate dielectric region involved in turning devices on and off. This typically refers to metal-oxide-semiconductor (MOS) devices such as capacitors, field-effect transistors (MOSFETs), or insulated-gate bipolar transistors (IGBTs). All presented examples are from MOS gated SiC devices. Specifically covered is time-dependent dielectric breakdown (TDDB) testing, with either constant-voltage stress (CVS), constant-current stress (CCS) or ramped voltage stress (RVS) / ramped current stress (RCS) for ramped breakdown (RBD) tests.

An issue related particularly to SiC substrates is their high defect density; which has been rapidly decreasing over time as substrate quality improves, but remains orders of magnitude higher than for silicon substrates. This, and the resulting high interface trap levels present at SiO₂/SiC interfaces, has in the past interfered with the understanding of the intrinsic properties of SiO₂ on SiC. Thus, in the testing guidelines presented here, the intrinsic properties of the oxides on SiC are themselves important to demonstrate/determine. Extrinsic failures can often be related to intrinsic material defects in the SiC wafer material, or to processing issues, and any mathematical treatment of extrinsic defects is beyond the scope of this document. For detailed analysis of early fail populations (See JESD74A). Of course, the testing recommended here is to allow determination of the intrinsic and extrinsic populations, specifically through analysis of the failure distributions. However, the reasons for extrinsic failures, and means to eliminate them, are not addressed here, but helpful experimental procedures to analyze extrinsic failures will be described.