



SLOVENSKI STANDARD
SIST EN 61691-2:2007

01-januar-2007

Vedenjski jeziki - 2. del: Večlogični sistem VHDL za model medobratovalnosti (IEC 61691-1:2001)

Behavioural languages -- Part 2: VHDL multilogic system for model interoperability

Verhaltens Ebenensprache -- Teil 2: System für mehrwertige Logik für das VHDL-Interoperabilitätsmodell

Langages relatifs au comportement -- Partie 2: Système multilogique en VHDL permettant l'interopérabilité des modèles

Ta slovenski standard je istoveten z: EN 61691-2:2001

ICS:

35.060

Jeziki, ki se uporabljajo v
informacijski tehniki in
tehnologiji

Languages used in
information technology

SIST EN 61691-2:2007

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EUROPEAN STANDARD

EN 61691-2

NORME EUROPÉENNE

EUROPÄISCHE NORM

December 2001

ICS 35.240.50

English version

Behavioural languages
Part 2: VHDL multilogic system for model interoperability
(IEC 61691-2:2001)

Langages relatifs au comportement
Partie 2: Système multilogique en VHDL
permettant l'interopérabilité des modèles
(CEI 61691-2:2001)

Verhaltensebenensprache
Teil 2: System für mehrwertige Logik
für das VHDL-Interoperabilitätsmodell
(IEC 61691-2:2001)

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Up-to-date lists and bibliographical references concerning such national standards may be obtained on application to the Central Secretariat or to any CENELEC member.

This European Standard exists in three official versions (English, French, German). A version in any other language made by translation under the responsibility of a CENELEC member into its own language and notified to the Central Secretariat has the same status as the official versions.

CENELEC members are the national electrotechnical committees of Austria, Belgium, Czech Republic, Denmark, Finland, France, Germany, Greece, Iceland, Ireland, Italy, Luxembourg, Malta, Netherlands, Norway, Portugal, Spain, Sweden, Switzerland and United Kingdom.

CENELEC

European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

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Ref. No. EN 61691-2:2001 E

Foreword

The text of document 93/130/FDIS, future edition 1 of IEC 61691-2, prepared by IEC TC 93, Design automation, was submitted to the IEC-CENELEC parallel vote and was approved by CENELEC as EN 61691-2 on 2001-09-01.

The following dates were fixed:

- latest date by which the EN has to be implemented at national level by publication of an identical national standard or by endorsement (dop) 2002-06-01
- latest date by which the national standards conflicting with the EN have to be withdrawn (dow) 2004-09-01

This standard is based on IEEE Std 1164:1993, Multivalued logic system for VHDL model interoperability.

Endorsement notice

The text of the International Standard IEC 61691-2:2001 was approved by CENELEC as a European Standard without any modification.

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INTERNATIONAL STANDARD

IEC 61691-2

First edition
2001-06

Behavioural languages –

**Part 2:
VHDL multilogic system
for model interoperability**

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BEHAVIOURAL LANGUAGES –

Part 2: VHDL multilogic system for model interoperability

FOREWORD

- 1) The IEC (International Electrotechnical Commission) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of the IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, the IEC publishes International Standards. Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. The IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
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International Standard IEC 61691-2 has been prepared by IEC technical committee 93: Design automation.

This standard is based on IEEE Std 1164-1993: *Multivalued logic system for VHDL model interoperability*

The text of this standard is based on the following documents:

FDIS	Report on voting
93/130/FDIS	93/140/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This standard does not follow the rules for the structure of international standards given in Part 3 of the ISO/IEC Directives.

IEC 61691 consists of the following parts, under the general title: *Behavioural languages*:

IEC 61691-1:1997, VHDL language reference manual ¹⁾

IEC 61691-2:2001, Part 2: VHDL multilogic system for model interoperability

¹⁾ The edition 2 with the title: VHSIC hardware description language VHDL (076a) (under consideration) will replace it.

IEC 61691-3-1, Part 3-1: Analog description in VHDL (under consideration)

IEC 61691-3-2:2001, Part 3-2: Mathematical operation in VHDL

IEC 61691-3-3:2001, Part 3-3: Synthesis in VHDL

IEC 61691-3-4, Part 3-4: Timing expressions in VHDL (under consideration)

IEC 61691-3-5, Part 3-5: Library utilities in VHDL (under consideration)

The committee has decided that the contents of this publication will remain unchanged until 2004. At this date, the publication will be

- reconfirmed;
- withdrawn;
- replaced by a revised edition, or
- amended.

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