SLOVENSKI STANDARD
SIST EN IEC 60749-26:2026

01-april-2026

Nadomešča:
SIST EN IEC 60749-26:2018

Polprevodniški elementi - Metode za mehansko in klimatsko preskušanje - 26. del: Preskušanje občutljivosti na elektrostatično razelektritev (ESD) - Model človeškega telesa (HBM) (IEC 60749-26:2025)

Semiconductor devices - Mechanical and climatic test methods - Part 26: Electrostatic discharge (ESD) sensitivity testing - Human body model (HBM) (IEC 60749-26:2025)

Halbleiterbauelemente - Mechanische und klimatische Prüfverfahren - Teil 26: Prüfung der Empfindlichkeit gegen elektrostatische Entladungen (ESD) - Human Body Model (HBM) (IEC 60749-26:2025)

Dispositifs à semiconducteurs - Méthodes d'essais mécaniques et climatiques - Partie 26: Essai de sensibilité aux décharges électrostatiques (DES) - Modèle du corps humain (HBM) (IEC 60749-26:2025)

Ta slovenski standard je istoveten z: **EN IEC 60749-26:2026**

ICS:

19.020	Preskuševalni pogoji in postopki na splošno	Test conditions and procedures in general
31.080.01	Polprevodniški elementi (naprave) na splošno	Semiconductor devices in general

SIST EN IEC 60749-26:2026 **en**

EUROPEAN STANDARD
NORME EUROPÉENNE
EUROPÄISCHE NORM

EN IEC 60749-26

February 2026

ICS 31.080.01

Supersedes EN IEC 60749-26:2018

English Version

Semiconductor devices - Mechanical and climatic test methods - Part 26: Electrostatic discharge (ESD) sensitivity testing - Human body model (HBM) (IEC 60749-26:2025)

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(IEC 60749-26:2025)

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CENELEC
European Committee for Electrotechnical Standardization
Comité Européen de Normalisation Electrotechnique
Europäisches Komitee für Elektrotechnische Normung

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Ref. No. EN IEC 60749-26:2026 E

European foreword

The text of document 47/2963/FDIS, future edition 5 of IEC 60749-26, prepared by TC 47 "Semiconductor devices" was submitted to the IEC-CENELEC parallel vote and approved by CENELEC as EN IEC 60749-26:2026.

The following dates are fixed:

• latest date by which the document has to be implemented at national level by publication of an identical national standard or by endorsement	(dop)	2027-02-28
• latest date by which the national standards conflicting with the document have to be withdrawn	(dow)	2029-02-28

This document supersedes EN IEC 60749-26:2018 and all of its amendments and corrigenda (if any).

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Endorsement notice

The text of the International Standard IEC 60749-26:2025 was approved by CENELEC as a European Standard without any modification.

In the official version, for Bibliography, the following notes have to be added for the standard indicated:

IEC 60749-26	NOTE	Approved as EN IEC 60749-26
IEC 60749-27	NOTE	Approved as EN 60749-27
IEC 60749-28	NOTE	Approved as EN IEC 60749-28

IEC 60749-26

Edition 5.0 2025-12

INTERNATIONAL STANDARD

Semiconductor devices - Mechanical and climatic test methods - Part 26: Electrostatic discharge (ESD) sensitivity testing - Human body model (HBM)

IEC 60749-26:2025-12(en)

ICS 31.080.01 ISBN 978-2-8327-0918-4

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

Semiconductor devices - Mechanical and climatic test methods - Part 26: Electrostatic discharge (ESD) sensitivity testing - Human body model (HBM)

FOREWORD

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IEC 60749-26 has been prepared by IEC technical committee 47: Semiconductor devices in collaboration with technical committee 101: Electrostatics. It is an International Standard.

This fifth edition cancels and replaces the fourth edition published in 2018. This edition constitutes a technical revision. This standard is based upon ANSI/ESDA/JEDEC JS-001-2023. It is used with permission of the copyright holders, ESD Association and JEDEC Solid state Technology Association.

This edition includes the following significant technical changes with respect to the previous edition:

a) new definitions have been added;

b) text has been added to clarify the designation of and allowances resulting from "low parasitics". The new designation includes the maximum number of pins of a device that can pass the test procedure.

The text of this International Standard is based on the following documents:

Draft	Report on voting
47/2963/FDIS	47/2984/RVD

Full information on the voting for its approval can be found in the report on voting indicated in the above table.

The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/publications.

A list of all parts in the IEC 60749 series, published under the general title *Semiconductor devices - Mechanical and climatic test methods*, can be found on the IEC website.

The committee has decided that the contents of this document will remain unchanged until the stability date indicated on the IEC website under webstore.iec.ch in the data related to the specific document. At this date, the document will be

- reconfirmed,
- withdrawn, or
- revised.

1 Scope

This part of IEC 60749 establishes the procedure for testing, evaluating, and classifying components and microcircuits in accordance with their susceptibility (sensitivity) to damage or degradation by exposure to a defined human body model (HBM) electrostatic discharge (ESD).

The purpose of this document is to establish a test method that will replicate HBM failures and provide reliable, repeatable HBM ESD test results from tester to tester, regardless of component type. Repeatable data will allow accurate classifications and comparisons of HBM ESD sensitivity levels.

ESD testing of semiconductor devices is selected from this test method, the machine model (MM) test method (see IEC 60749-27) or other ESD test methods in the IEC 60749 series. Unless otherwise specified, this test method is the one selected.

2 Normative references

There are no normative references in this document.

3 Terms and definitions

For the purposes of this document, the following terms and definitions apply.

ISO and IEC maintain terminology databases for use in standardization at the following addresses:

- IEC Electropedia: available at https://www.electropedia.org/
- ISO Online browsing platform: available at https://www.iso.org/obp

3.1
above-passivation layer
APL
low-impedance metal plane built on the surface of a die, above the passivation layer, which connects a group of bumps or pins

Note 1 to entry This structure is sometimes referred to as a redistribution layer (RDL). There can be multiple APLs (sometimes referred to as islands) for a power or ground group.

Note 2 to entry: The group of bumps or pins is typically a power group or a ground group.

3.2
cloned non-supply pin
set of input, output or bidirectional pins using the same I/O cell and electrical schematic and sharing the same associated supply pin group(s) including ESD power clamp(s)

3.3
component
item such as a resistor, diode, transistor, integrated circuit (IC) or hybrid circuit

3.4
component failure
condition in which a tested component does not meet one or more specified static or dynamic data sheet parameters

3.5
coupled non-supply pin pair
two pins that have an intended direct current path (such as a pass gate or resistors, such as differential amplifier inputs, or low voltage differential signalling (LVDS) pins), including analogue and digital differential pairs and other special function pairs (e.g. D+/D−, XTALin/XTALout, RFin/RFout, TxP/TxN, RxP/RxN, CCP_DP/CCN_DN, etc.)

3.6
data sheet parameters
static and dynamic component performance data supplied by the component manufacturer or supplier

3.7
ESD withstand voltage
withstand threshold
highest voltage level not causing device failure with the device passing all tests performed at lower voltage levels

Note 1 to entry: See note under 'failure window' definition

3.8
exposed pad
exposed metal plate on an IC package

Note 1 to entry: This metal plate can be electrically connected to the die.

3.9
feedthrough
direct or indirect (via a series resistor) connection from a pad cell layout

Note 1 to entry: This connection can allow additional elements, not included in the pad cell, to make electrical connections to the bond pad (see Annex A).

3.10
failure window
intermediate range of stress voltages that can induce failure in a particular device type, when the device type can pass some stress voltages both higher and lower than this range

Note 1 to entry: A component with a failure window can pass a 500 V test, fail a 1 000 V test and pass a 2 000 V test. The withstand voltage of such a device is 500 V.

3.11
human body model electrostatic discharge
HBM ESD
ESD event meeting the waveform criteria specified in this document, approximating the discharge from the fingertip of a typical human being to a grounded device

3.12
HBM ESD tester
HBM simulator
equipment that applies an HBM ESD to a component

3.13
I_{ps}
peak current value determined by the current at time t_{max} on the linear extrapolation of the exponential current decay curve, based on the current waveform data over a 40 nanosecond period beginning at t_{max}

SEE: Figure 2 a).

3.14
I_{psmax}

highest current value measured including the overshoot or ringing components due to internal test simulator RLC parasitics

SEE: Figure 2 a).

3.15
no connect pin

package interconnection that is not electrically connected to a die

EXAMPLE Pin, bump, ball interconnection.

Note 1 to entry: There are some pins which are labelled as no connect, which are actually connected to the die and should not be classified as a no connect pin.

3.16
non-socketed tester

HBM simulator that makes contact to the device under test (DUT) pins (or balls, lands, bumps or die pads) with test probes rather than placing the DUT in a socket

3.17
non-supply pin

pin that is not categorized as a supply pin or no connect pin

Note 1 to entry This includes pins such as input, output, offset adjusts, compensation, clocks, controls, address, data, Vref pins and VPP pins on EPROM memory. Most non-supply pins transmit or receive information such as digital or analogue signals, timing, clock signals, and voltage or current reference levels.

3.18
package plane

low impedance metal layer built into an IC package connecting a group of bumps or pins (typically power or ground)

Note 1 to entry: There can be multiple package planes (sometimes referred to as islands) for each power and ground group.

3.19
pin

terminal, land, lead, bump, ball, or exposed pad on the package that can make an electrical connection to the die

3.20
pre-pulse voltage

voltage occurring at the device under test (DUT) just prior to the generation of the HBM current pulse

Note 1 to entry: See Clause C.2.

3.21
pulse generation circuit

dual polarity pulse source circuit network that produces a human body discharge current waveform

Note 1 to entry The circuit network includes a pulse generator with its test equipment internal path up to the contact pad of the test fixture. This circuit is also referred to as dual polarity pulse source.

3.22
ringing

high frequency oscillation superimposed on a waveform

3.23
shorted non-supply pin
any non-supply pin (typically an I/O pin) that is metallically connected (typically < 3 Ω) on the chip or within the package to another non-supply pin (or set of non-supply pins)

3.24
socketed tester
HBM simulator that makes contact to DUT pins (or balls, lands, bumps or die pads) using a DUT socket mounted on a test fixture board

3.25
specification limit
SPL
target specification level set by the customer's requirements or internal target

Note 1 to entry: See Annex A.

3.26
spurious current pulse
small HBM shaped pulse that follows the main current pulse, and is typically defined as a percentage of I_{psmax}

3.27
step-stress hardening
ability of a component subjected to increasing ESD voltage stresses to withstand higher stress levels than a similar component not previously stressed

EXAMPLE: A component can fail at 1 000 V if subjected to a single stress, but fail at 3 000 V if stressed incrementally from 250 V.

3.28
supply pin
any pin that provides current to a circuit

Note 1 to entry: Supply pins typically transmit no information (such as digital or analogue signals, timing, clock signals, and voltage or current reference levels). For the purpose of ESD testing, power and ground pins are treated as supply pins.

3.29
terminal
output (A) or return (B) of the simulator pulse source

3.30
tester channel
path connecting the pulse source of the simulator to the DUT pin

3.31
test fixture board
specialized circuit board, with one or more component sockets, which connects the DUT(s) to the HBM simulator

3.32
t_{max}
time when I_{ps} is at its maximum value (I_{psmax})

SEE: Figure 2.

3.33
trailing current pulse
current pulse that occurs after the HBM current pulse has decayed

Note 1 to entry: See Clause C.2.

Note 2 to entry: A trailing current pulse is a relatively constant current often lasting for hundreds of microseconds.

3.34
V_1
maximum HBM stress voltage step where all of the selected cloned non-supply pins pass

Note 1 to entry: See Annex A.

3.35
V_2
minimum HBM stress voltage step where all the selected cloned non-supply pins fail

Note 1 to entry: See Annex A.

3.36
V_M
minimum HBM stress voltage step where 50 % or greater of the selected cloned non-supply pins fail

Note 1 to entry: See Annex A.

4 Apparatus and required equipment

4.1 Waveform verification equipment

All equipment used to evaluate the tester shall be calibrated in accordance with the manufacturer's recommendation. This includes the oscilloscope, current probe and high voltage resistor load. Maximum time between calibrations shall be one year. Calibration shall be traceable to national or international standards.

Equipment capable of verifying the pulse waveforms defined in the test method in this document includes, but is not limited to, an oscilloscope, evaluation loads and a current probe.

4.2 Oscilloscope

A digital oscilloscope should be preferred but analogue oscilloscopes may also be used. In order to ensure accurate current waveform capture, the oscilloscope shall meet the following requirements:

a) minimum sensitivity of 100 mA per major division when used in conjunction with the current probe as specified in 4.4;
b) minimum bandwidth of 350 MHz;
c) for analogue scopes, minimum writing rate of one major division per nanosecond.