



SLOVENSKI STANDARD SIST-TP CEN/CLC/TR 18202:2025

01-november-2025

Slojni model kvantnega računalništva

Layer model of Quantum Computing

Schichtenmodell des Quantencomputings

Modèle en couches de l'informatique quantique

Ta slovenski standard je istoveten z: CEN/CLC/TR 18202:2025

ICS:

35.020

Informacijska tehnika in
tehnologija na splošno

Information technology (IT) in
general

SIST-TP CEN/CLC/TR 18202:2025

en,fr,de

TECHNICAL REPORT

CEN/CLC/TR 18202

RAPPORT TECHNIQUE

TECHNISCHER REPORT

September 2025

ICS 35.020

English version

Layer model of Quantum Computing

Modèle en couches de l'informatique quantique

Schichtenmodell des Quantencomputings

This Technical Report was approved by CEN on 11 August 2025. It has been drawn up by the Technical Committee CEN/CLC/JTC 22.

CEN and CENELEC members are the national standards bodies and national electrotechnical committees of Austria, Belgium, Bulgaria, Croatia, Cyprus, Czech Republic, Denmark, Estonia, Finland, France, Germany, Greece, Hungary, Iceland, Ireland, Italy, Latvia, Lithuania, Luxembourg, Malta, Netherlands, Norway, Poland, Portugal, Republic of North Macedonia, Romania, Serbia, Slovakia, Slovenia, Spain, Sweden, Switzerland, Türkiye and United Kingdom.

iTeh Standards
(<https://standards.iteh.ai>)
Document Preview

[SIST-TP CEN/CLC/TR 18202:2025](https://standards.iteh.ai/catalog/standards/sist/8f3e1594-83e1-480e-9fa6-c5429b7137f4/sist-tp-cen-clc-tr-18202-2025)<https://standards.iteh.ai/catalog/standards/sist/8f3e1594-83e1-480e-9fa6-c5429b7137f4/sist-tp-cen-clc-tr-18202-2025>

CEN-CENELEC Management Centre:
Rue de la Science 23, B-1040 Brussels

Contents

Page

European foreword	3
Introduction	4
1 Scope.....	5
2 Normative references.....	5
3 Terms and definitions.....	5
4 Abbreviations.....	6
5 Overview	6
6 Low level hardware and control layers	8
6.1 Cryogenic solid state.....	8
6.1.1 General.....	8
6.1.2 Layer 1 – Quantum devices.....	8
6.1.3 Layer 2 – Control highway	8
6.1.4 Layer 3 – Control electronics.....	9
6.1.5 Layer 4 – Control software.....	9
6.2 Room temperature solid state	10
6.3 Trapped ions.....	10
6.4 Neutral atoms.....	11
6.5 Photonic quantum computing.....	11
6.6 Other architectures.....	11
7 Hardware abstraction layer (HAL)	12
7.1 General.....	12
7.2 Organization of qubits.....	12
7.3 The concept of native gates	12
7.4 Concept of primitive gates.....	14
7.5 Concept of measurement	15
7.6 Interfacing considerations	15
8 Assembly layer.....	15
9 Programming layer	15
9.1 General.....	15
9.2 Programming languages and libraries.....	15
9.3 Quantum compilation.....	16
10 Service layer	16
11 Communication unit	17
11.1 General.....	17
11.2 Example information flow	17
11.2.1 Single user accessing the full quantum stack	17
11.2.2 Multiple users accessing the full quantum stack.....	18
11.2.3 User accessing lower layer	18
Bibliography	19